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Connecting the Future

MT6771 PCB Design Guidelines V0.2

2017/09/29

Revision History

Version	Date	Description	Editors
V0.1	2017/09/15	First release	Tina Tang, YH Ku, Wanda Tseng, Sean Hwang, PS Chen, FK Pan, Charles Chen
V0.2	2017/09/29	Modify LP3 layout guideline	Tina Tang, Sean Hwang

Outlines

- **Packaging**
  - Package outline of MT6771
  - MT6771 footprint recommendation
  - MT6771 ball out design
- **General Guidelines**
  - PCB stack-up recommendation
  - Placement notes
- **Design Guidelines for High-Speed Digital Signals**
  - LPDDR4X/LPDDR3
  - PDN design
- **Others**
  - MT6177 (RF transceiver)
  - MT6358 (PMU)
  - MT6631 (BT/FM/Wi-Fi/GPS)
  - MT6370 (Battery Charger/USB_PD)
  - eMMC/USB/MIPI/SIM Card/T-Card

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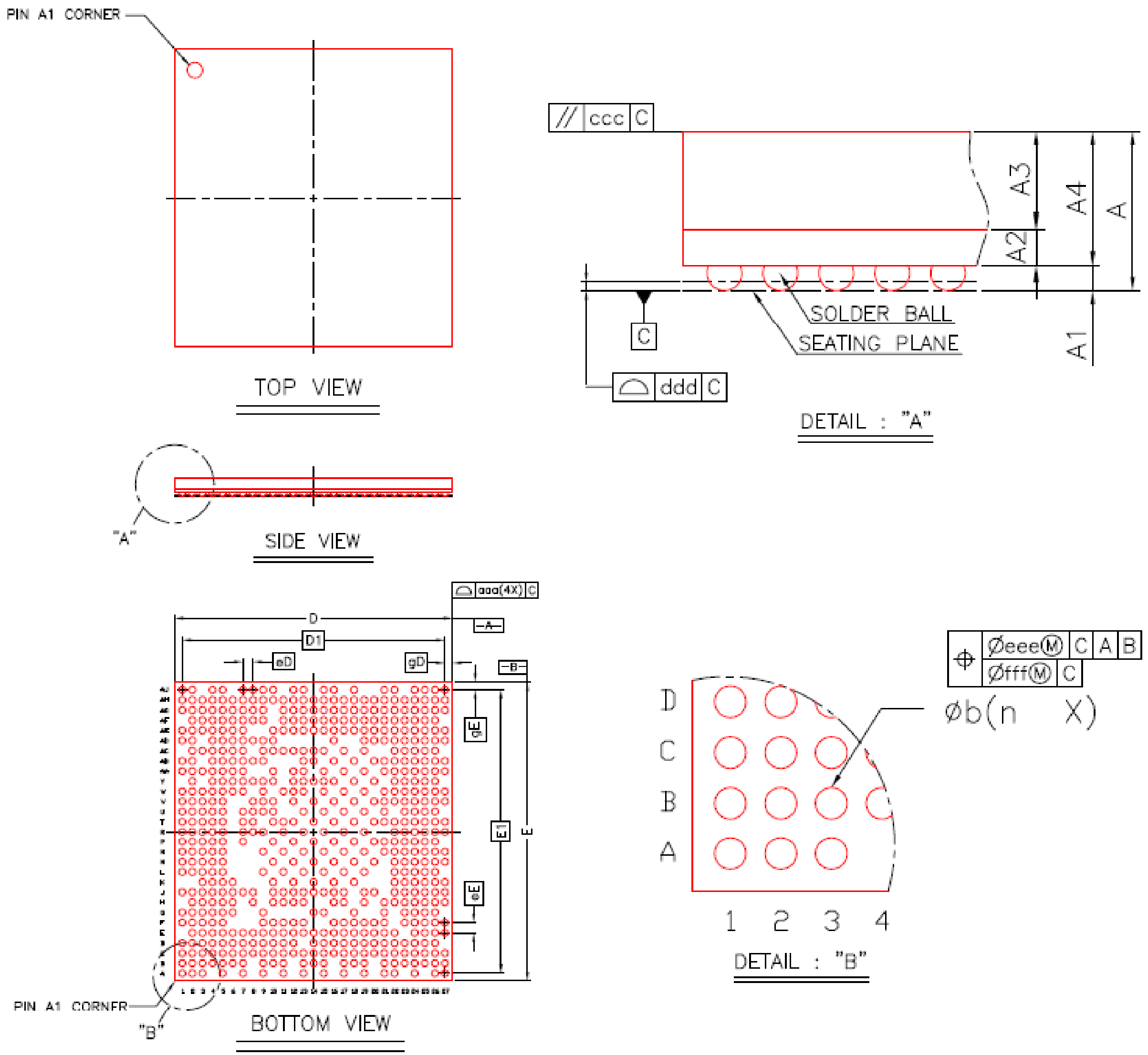
Package Outline of MT6771



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	10.9	11.0	11.1
	Y	E	11.7	11.8	11.9
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.45 Ref.	
Substrate Thickness		A2		0.141 Ref.	
Substrate+Mold Thickness		A4	0.541	0.591	0.641
Total Thickness		A	–	–	0.90
Ball Diameter				0.25	
Ball Stand Off		A1	0.14	0.18	0.22
Ball Width		b	0.22	0.27	0.32
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		599	
Edge Ball Center to Center	X	D1		10.40	
	Y	E1		11.20	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

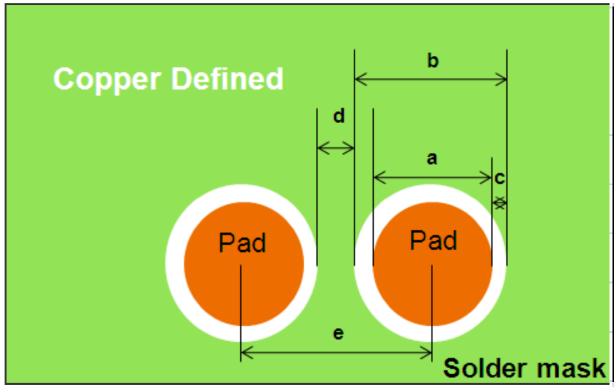
MT6771 Footprint Recommendation

Note:

- Use **copper defined** for all solder pads (see Figure 1).
- Recommended stencil opening ➔ 0.24mm square with 0.075R angle (see green area in Figure 2)
- **Use 0.1/0.22mm (drill/land) laser via on PAD to improve the yield of SMT.**

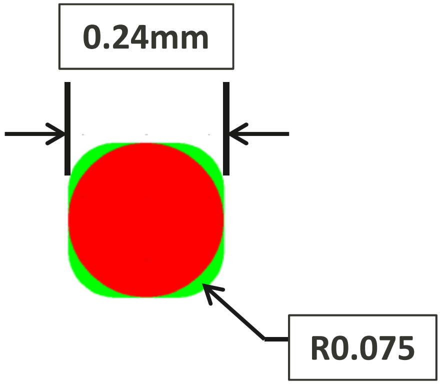
As in Figure 1, use **copper defined** for all pins.
Pad size: 0.24mm; solder mask: 0.315mm

Figure 1

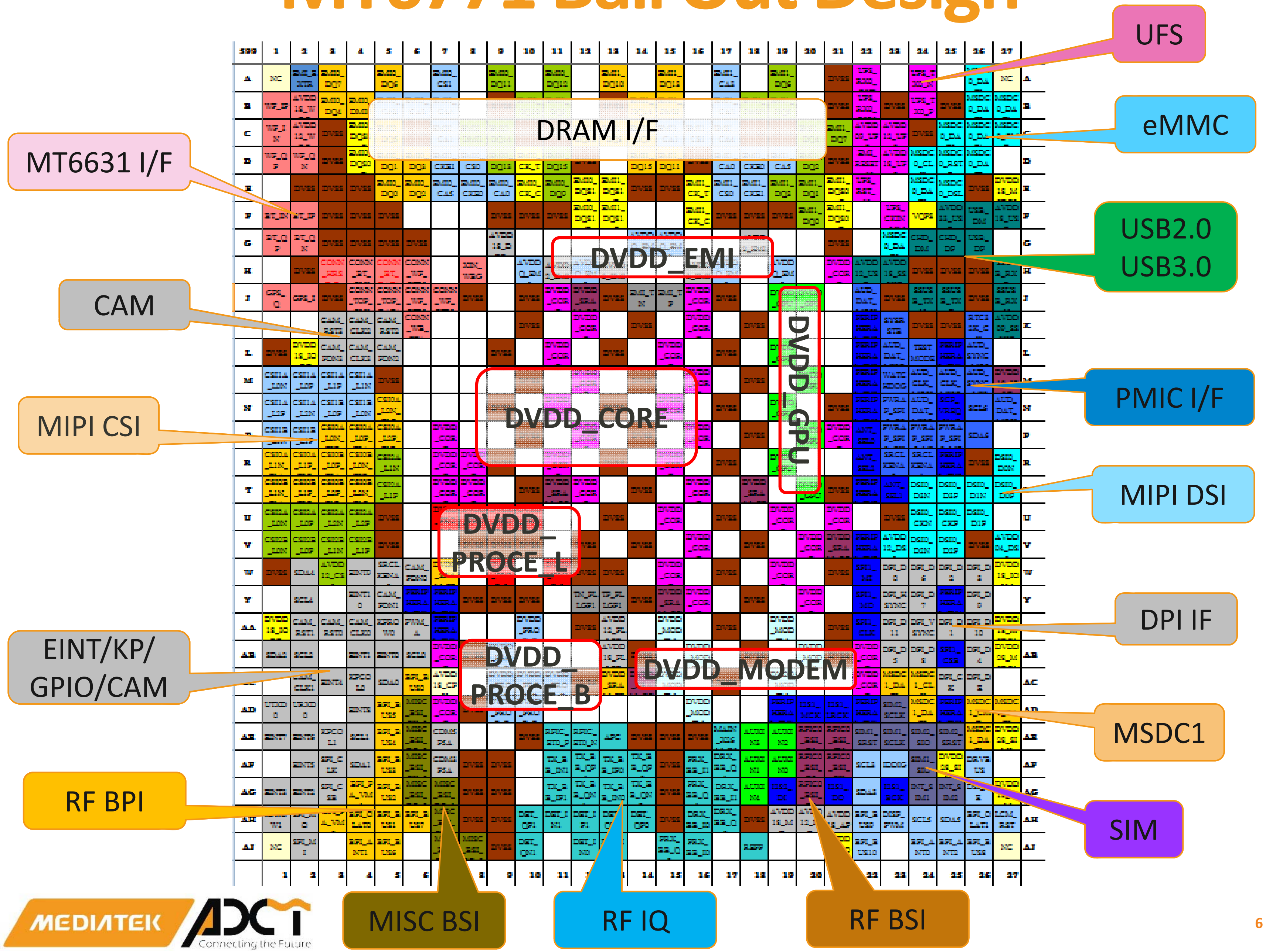


Copper defined PCB land pad and Solder mask opening rule		
Land pad size	a	0.24mm
Sloder mask opening	b	a+0.075mm
Solder mask clearance	c	0.0375mm
Solder dam	d	0.085mm
Ball pitch	e	0.4mm

Figure 2



MT6771 Ball Out Design



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PCB Stack-up Recommendation

- To keep the best power integrity, the total thickness of PCB should be < 0.7mm.
- Follow the relative stack-up arrangement listed on the following pages for LPDDR4 and power distribution network.
- Others signals can be routed in the rest of the area.
- Two types of stack-up are recommended here. For other combinations, extend from it.
  - 8 Layer HDI2
  - 10 Layer HDI2

PCB Stack-up: 8-layer HDI2

0.7mm, double side

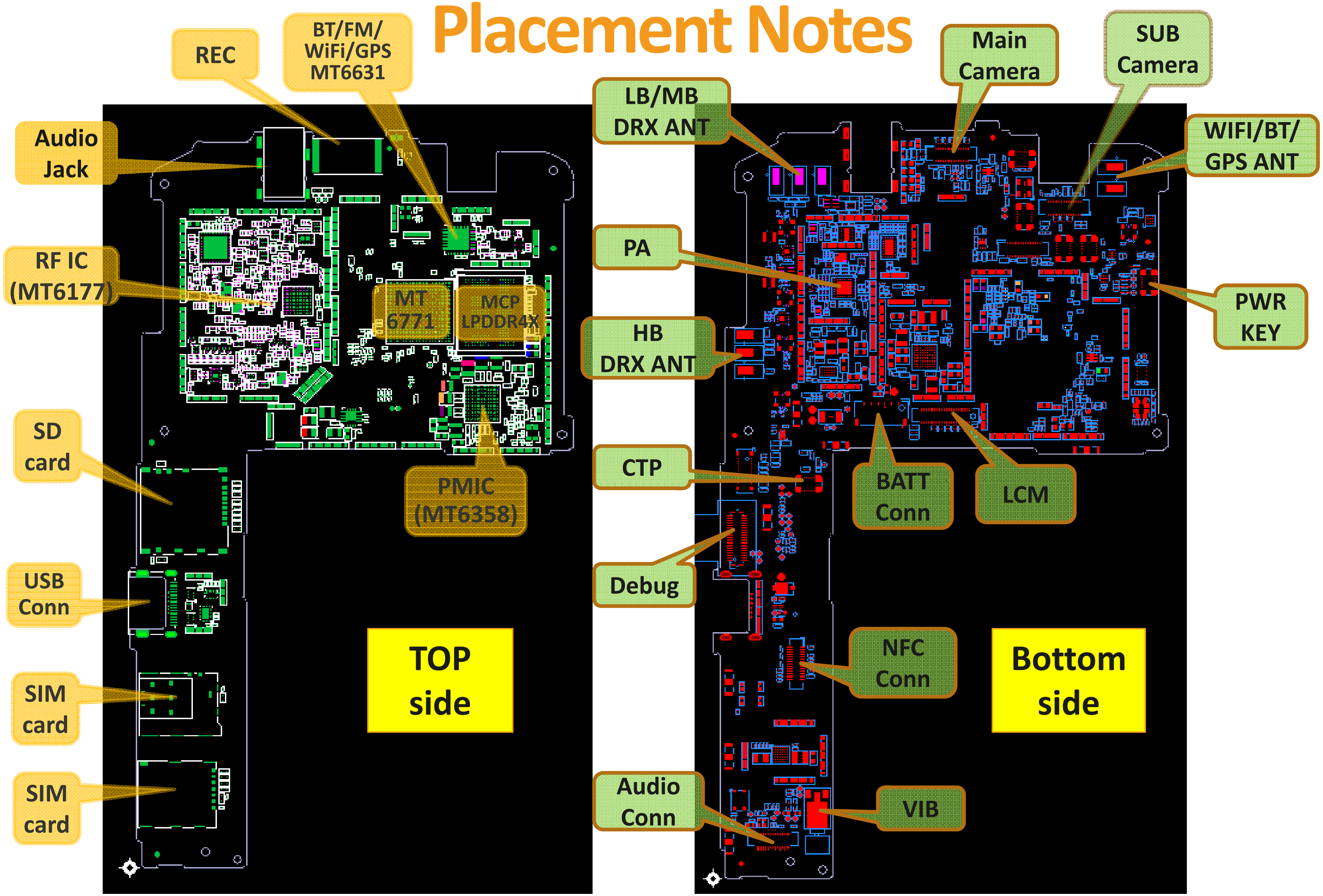
Layer name	Layer type	Theoretical thickness (mm)	Theoretical thickness (mil)	ER	Layer Definition S/P/G				
					PORC	GPU	CORE	MODEM	DDR
S/M	Solder mask	0.020	0.787	3.3					
TOP	1/3oz+plating	0.025	0.984						S
	Prepreg	0.050	1.969	3.5					
L2	1/3oz+plating	0.019	0.748						G
	Prepreg	0.050	1.969	3.3					
L3	1/3oz+plating	0.022	0.866						S
	Prepreg	0.075	2.953	3.3					
L4	H oz	0.015	0.591						G
	core	0.150	5.906	3.3					
L5	H oz	0.015	0.591			P	P	P	P
	Prepreg	0.075	2.953	3.3					
L6	1/3oz+plating	0.022	0.866		G	G	G	G	G
	Prepreg	0.050	1.969	3.3					
L7	1/3oz+plating	0.019	0.748		P				
	Prepreg	0.050	1.969	3.3					
BOT	1/3oz+plating	0.025	0.984						
S/M	Solder mask	0.020	0.787	3.3					
		0.702	27.638						

PCB Stack-up: 10-layer HDI2

0.7mm, double side

Layer name	Layer type	Theoretical thickness (mm)	Theoretical thickness (mil)	ER	Layer Definition S/P/G				
					PORC	GPU	CORE	MODEM	DDR
S/M	Solder mask	0.030	1.181	3.3					
TOP	1/3oz+plating	0.025	0.984						S
	Prepreg	0.050	1.969	3.5					
L2	1/3oz+plating	0.022	0.866						G
	Prepreg	0.050	1.969	3.3					
L3	1/3oz+plating	0.022	0.866						S
	Prepreg	0.050	1.969	3.3					
L4	H oz	0.015	0.591						G
	core	0.060	2.362	3.3					
L5	H oz	0.015	0.591			P	P	P	P
	Prepreg	0.050	1.969	3.3					
L6	H oz	0.015	0.591			G	G	G	G
	core	0.060	2.362	3.3					
L7	H oz	0.015	0.591		P				
	Prepreg	0.050	1.969	3.3					
L8	1/3oz+plating	0.022	0.866		G				
	Prepreg	0.050	1.969	3.3					
L9	1/3oz+plating	0.022	0.866						
	Prepreg	0.050	1.969	3.5					
BOT	1/3oz+plating	0.025	0.984						
S/M	Solder mask	0.030	1.181	3.3					
		0.708	27.874						

Placement Notes



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PCB Module Design

MMD
MediaTek Module Design

- **We recommend you adopt modules by MediaTek as the first priority.**

As the design trend turns to developing light, thin and higher battery capacity on smart phones, the complexity on system design becomes a great challenge nowadays. It is a time and cost consuming process to meet the layout constraints and at the same time deliver a good signal and power integrity.

To help our customers to rapidly design a correct, performance-oriented and reliable layout on PCB, we have introduced the **MMD (MediaTek Module Design)** solution. MMD provides optimized CPU and MCP layout design with guaranteed performance and stability. Meanwhile, it greatly shortens the time to market.

The main purpose of MMD is providing a convenient and flexible solution. The ideal condition is to implant the modules without any modification. However, if the module cannot match your mechanics, you can still partially adopt MMD and enjoy the benefits from it.

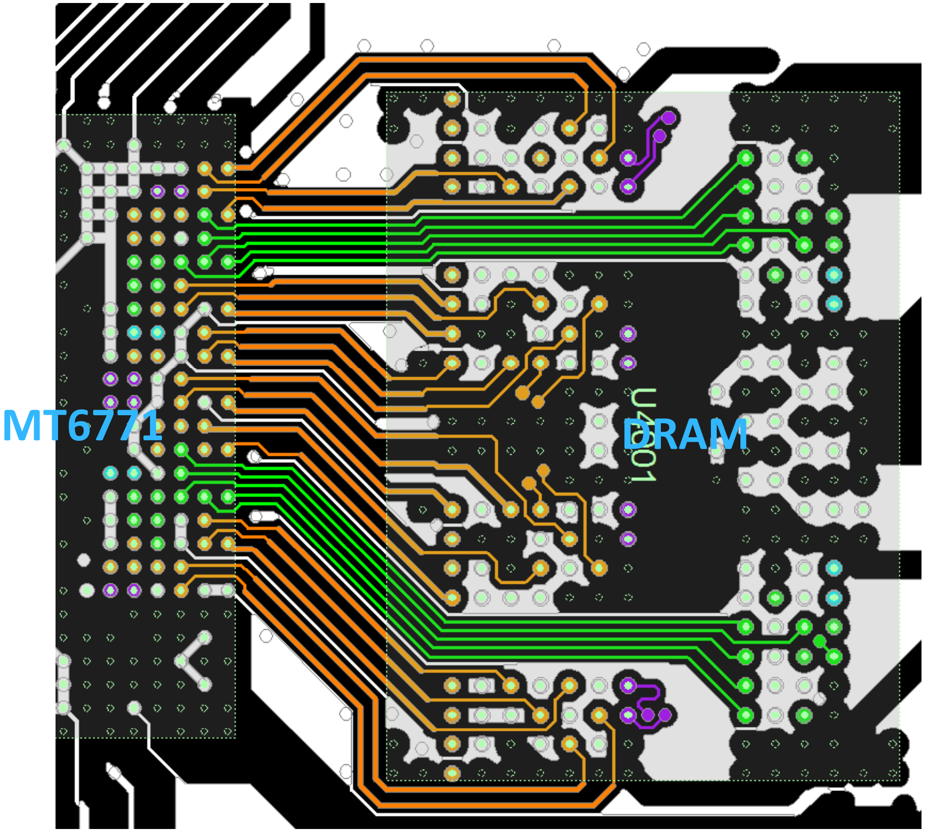
Contact your corresponding FAE when you have any problem in introducing MMD.

Enabling your High-speed Digital Design~

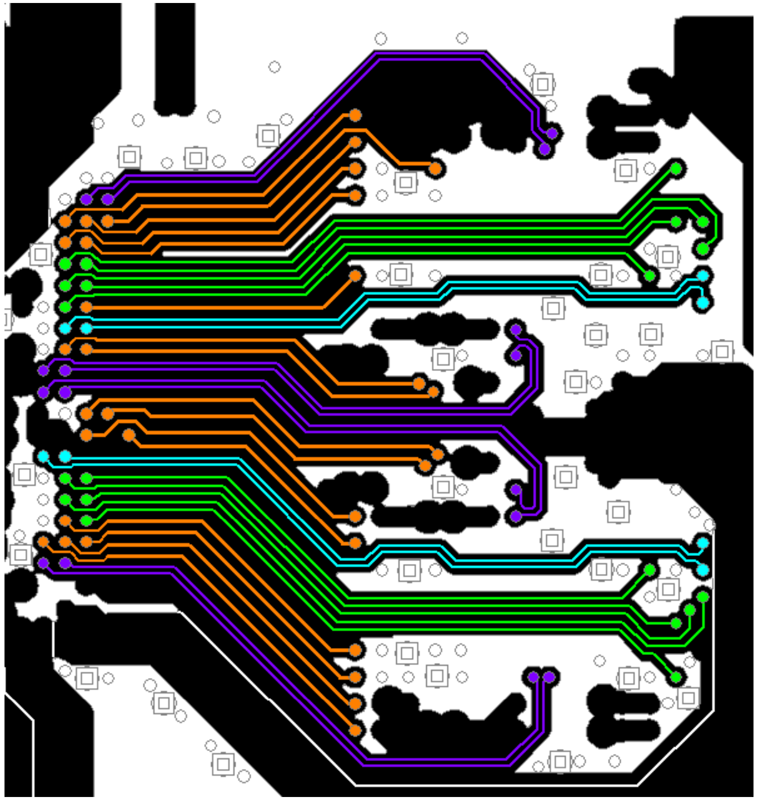
SIE (Signal Integrity Express): SI/PI simulation support

LPDDR4X - Placement

- Please keep the spacing between MT6771 and DRAM as small as possible.
- Recommend the spacing is less than 0.6mm.



L1



L3

DQ DQS CA CLK

LPDDR4X - Guideline

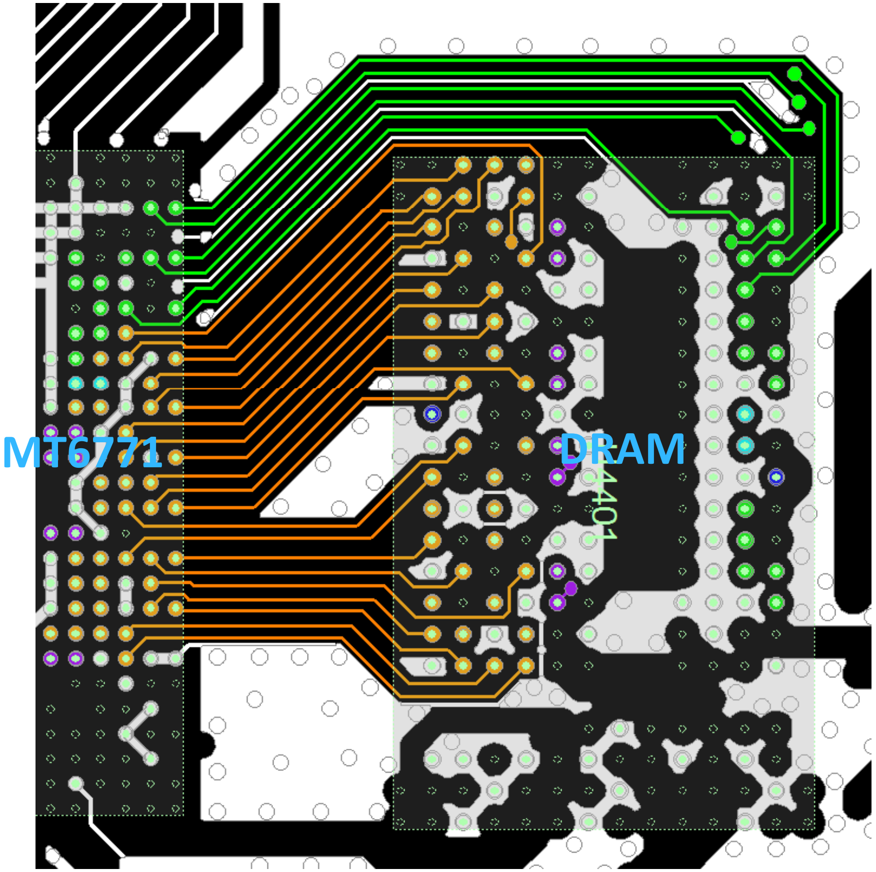
Grouping	Signal Name	#	Description
DQ	EMI[0:1]_DQ[0:15]	32	Data bus
	EMI[0:1]_DMI[0:1]	4	Data mask
CA	EMI[0:1]_CA[0:5]	12	Command/Address
	EMI[0:1]_CKE[0:1], EMI[0:1]_CS[0:1], EMI_RESET_N	9	Clock enable, Chip select, Reset
DQS	EMI[0:1]_DQS[0:1]_T, EMI[0:1]_DQS[0:1]_C	8	Data strobe
CLK	EMI[0:1]_CK_T, EMI[0:1]_CK_C	4	Clock

1. Please remove test point if not necessary
2. Place ground via when layer transition happens
3. It is not necessary to match routing length but keep trace length as short as possible.
4. For **LPDDR4X 3733**, recommend thickness of **Prepreg1-2 and Prepreg2-3** are less than **50um**.
5. Shielding traces on L1 must connect to ground plane on L2 and/or ground balls on L1 at both SoC side and DRAM side.

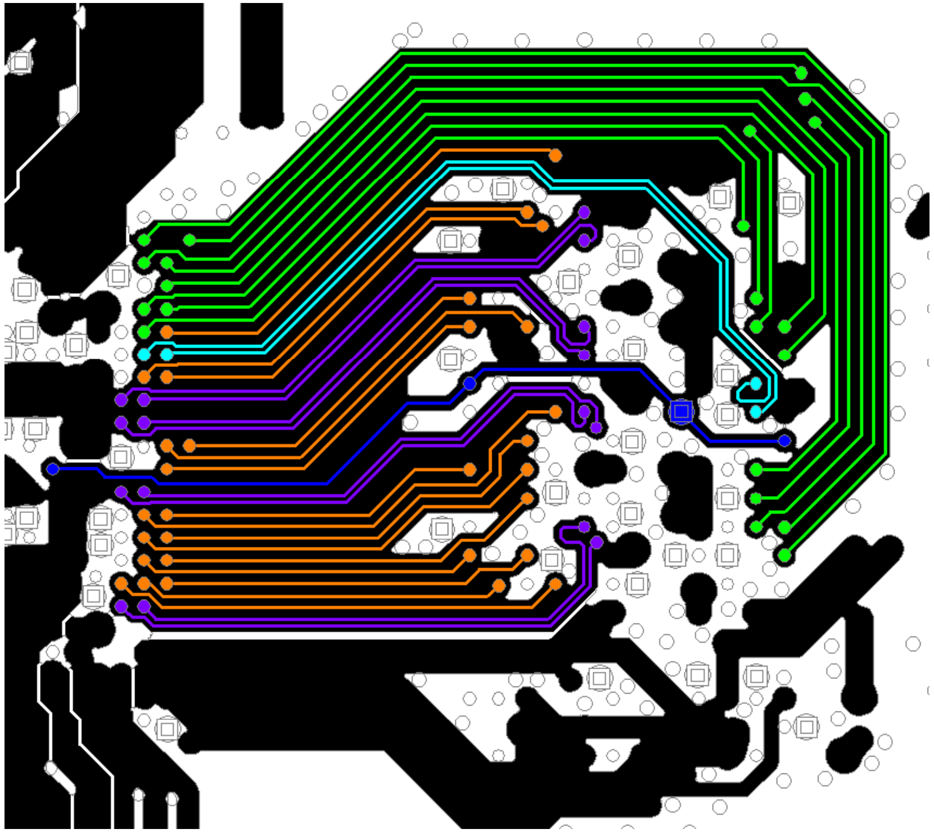
Group	Routing Layer	Reference	Shielding	Width(um)		Edge-to-edge Spacing(um)		Ground Spacing(um)	Intra Skew(um)
				Main Route	Breakout	Main Route	Breakout		
DQ	L1	L2	GSSSG	120	60	>150	>90	60	
	L3	L2, L4		75	60	>150	>80	60	
CA	L1	L2	Group	60	60	>90	>90	60	
	L3	L2, L4		60	60	>90	>80	60	
DQS/CLK	L3	L2, L4		60	60	>150	>80	60	<150

LPDDR3 - Placement

- Please keep the spacing between MT6771 and DRAM as small as possible.
- Recommend the spacing is less than 0.6mm.



L1



L3

DQ DQS CA CLK REF

LPDDR3 - Guideline

Grouping	Signal Name	#	Description
DQ	EMI0_DQ[0:31]	32	Data bus
	EMI0_DMI[0:3]	4	Data mask
CA	EMI0_CA[0:9]	10	Command/Address
	EMI0_CKE[0:1], EMI0_CS[0:1],	4	Clock enable, Chip select, Reset
DQS	EMI0_DQS[0:3]_T, EMI0_DQS[0:3]_C	8	Data strobe
CLK	EMI0_CK_T, EMI0_CK_C	2	Clock
REF	VREF_EMI	1	Reference voltage

1. Please remove test point if not necessary
2. Place ground via when layer transition happens
3. It is not necessary to match routing length but keep trace length as short as possible.
4. Shielding traces on L1 must connect to ground plane on L2 at both SoC side and DRAM side.

Group	Routing Layer	Reference	Shielding	Width(um)		Edge-to-edge Spacing(um)		Ground Spacing(um)	Intra Skew(um)
				Main Route	Breakout	Main Route	Breakout		
DQ	L1	L2		60	60	>120	>90	60	
	L3	L2, L4		60	60	>120	>80	60	
CA	L1	L2	GSSG	60	60	>150	>90	60	
	L3	L2, L4		60	60	>150	>80	60	
DQS/CLK	L3	L2, L4		60	60	>150	>80	60	<150
REF	L3	L2, L4		60	60	>150	>80	60	

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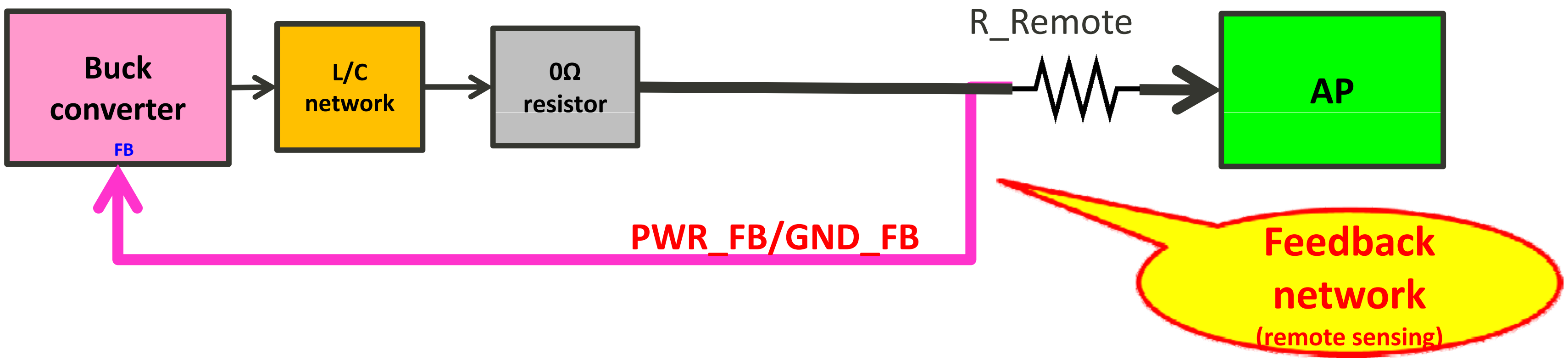
Basic Concepts of Power Delivery Network

- With the increasing demand of switching current and power consumption, the conventional PCB design concept is no longer sufficient in dealing with high-performance smart phone. Thus, a well-designed PDN (Power Delivery Network) on PCB is greatly significant for system stability and performance.
- The whole PDN should include all the interconnections and current return paths from PMIC to AP. The performance mainly depends on the location and number of power traces, PWR/GND vias, and decoupling capacitors. These parameters are defined in the following guidelines.

Ball List Table

Signal Name	#	Ball	Description
VPROC1 **(DVDD_PROC_B)**	7	AA10 AB9 AC9 AC10 AC11 AD9 AD10	Provides application processor CPU1 power
VPROC2 **(DVDD_PROC_L)**	6	U7 U8 U9 U10 W9 W11	Provides application processor CPU2 power
VGPU (**DVDD_GPU**)	8	J19 J20 L19 M20 N19 P20 R19 T20	Provides application processor GPU power.
VCORE (**DVDD_CORE**)	36	AB7 AB22 AC22 AD7 H21 J11 J16 K12 K16 L11 L15 M12 M16 N11 N15 P7 P12 P16 P21 R7 R8 R11 R15 T7 T8 T12 T16 U15 U21 V16 W15 Y16 V20 W19 Y20 U19	Provides application processor CORE power.
VMODEM (**DVDD_MODEM**)	7	AA15 AA19 AB16 AB20 AC15 AC19 AD16	Provides application processor MODEM power.
VEMI_VDD2 (**EMI_VDD2**)	4	G18 H11 H13 H16	Provides application processor EMI VDD2 power.
VEMI_VDDQ (**EMI_VDDQ**)	6	G14 G15 H10 H12 H17 H19	Provides application processor EMI VDDQ power.
VSRAM_PROC1 (**DVDD_SRAM_PROC_B**)	1	AC13	Provides application processor CPU1 SRAM power.
VSRAM_PROC2 (**DVDD_SRAM_PROC_L**)	1	W7	Provides application processor CPU2 SRAM power.
VSRAM_GPU (**DVDD_VSRAM_GPU_PMU**)	1	T18	Provides application processor GPU SRAM power.
VSRAM_CORE (**DVDD_SRAM_CORE**)	5	J12 T11 Y15 AC14 V21	Provides application processor CORE SRAM power.

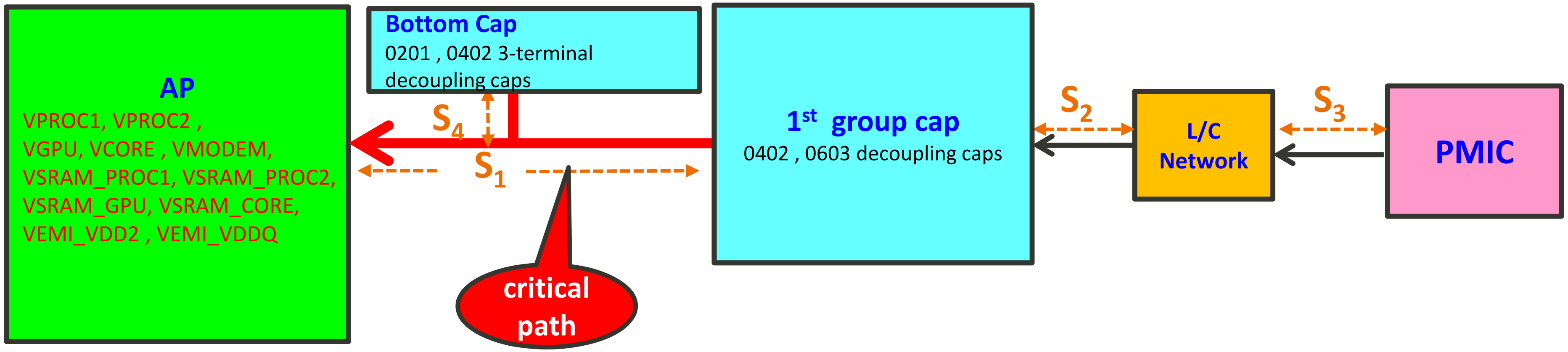
Guidelines for Remote Sensing



To compensate voltage loss, each two feedback paths (PWR_FB and GND_FB) are connected from every critical power domain which is close to MT6771 to the buck converter (PMIC).

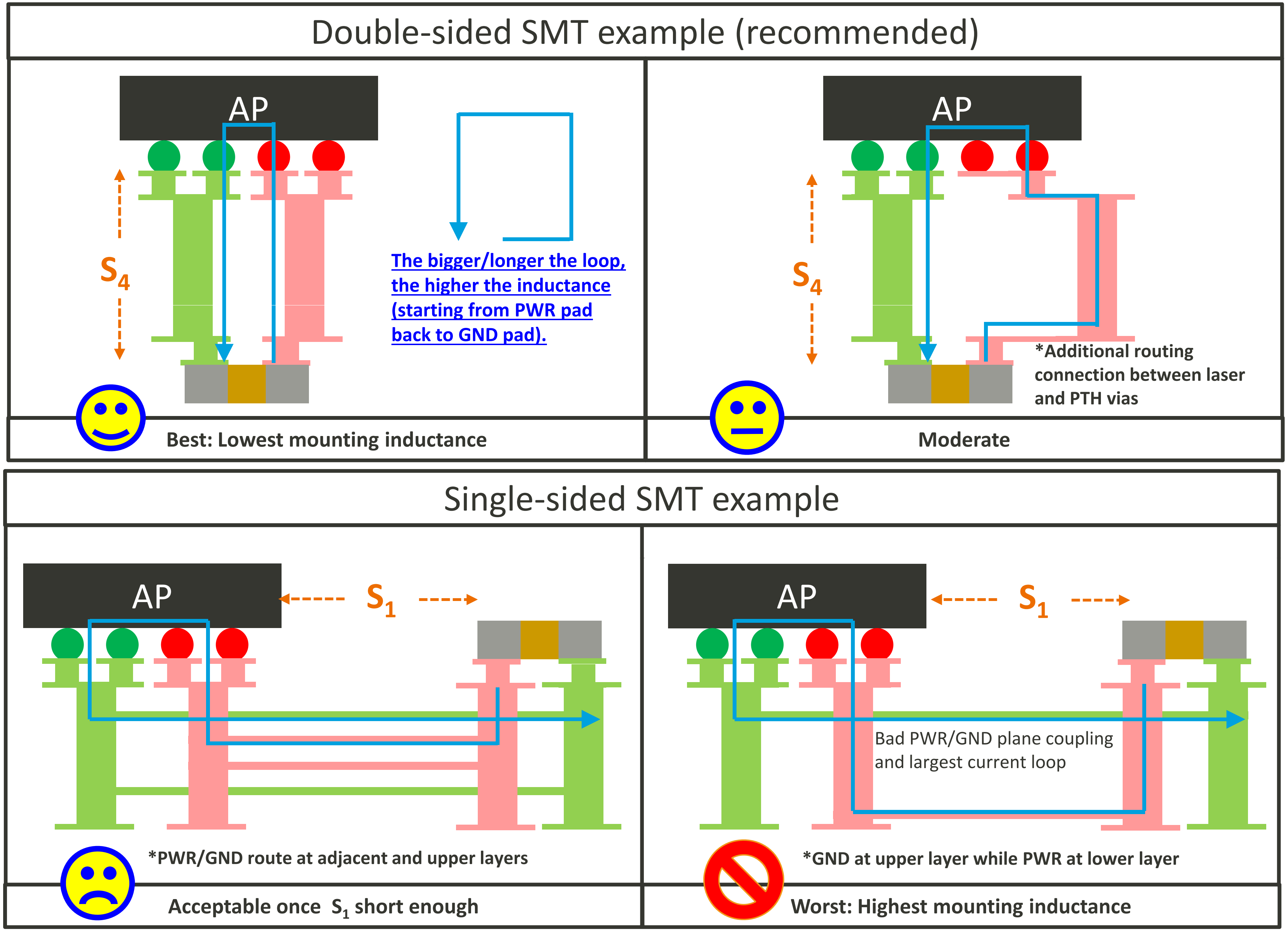
1. The voltage detection networks are sensitive to noise coupling. Use ground shielding for the entire trace including vias.
2. To keep the accuracy of feedback voltage, do not move the connection away from the bottom of AP and follow the resistance(R_Remote) spec.

Guidelines for Power Domain

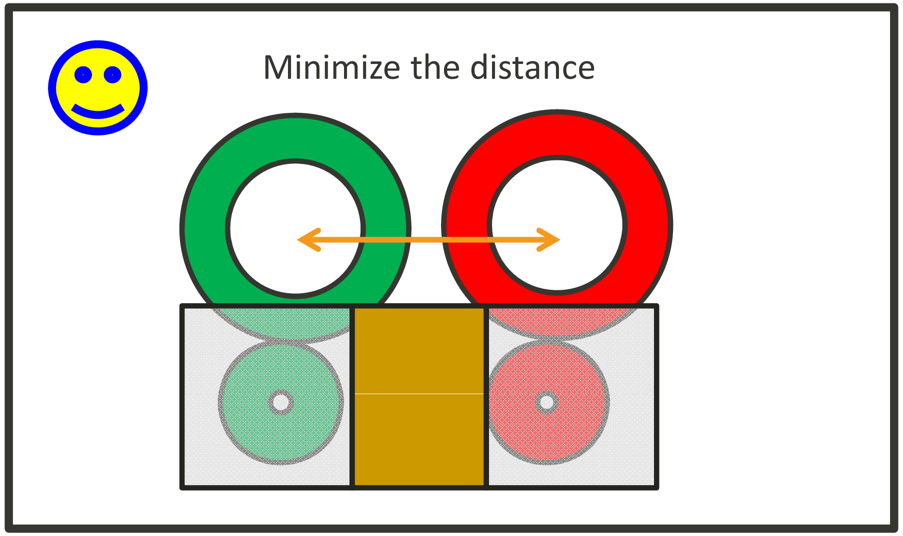


1. The whole PDN is from PMIC output pin, through (the LC low-pass filter) & decoupling caps to AP. PDN is the source of all switching currents.
2. "Critical-Path" is defined as the power trace segment from the 1st group cap to AP. The critical path design should follow the given PCB layout guidelines.
3. 2-sided SMT:
   1) In the "bottom cap" region, place 0201 and 0402 SMD capacitors right underneath the power balls. In "1st group cap" region, place the rest of decoupling caps.
   2) S_1 is defined as the critical path from "1st group cap" to AP. The corresponding PCB routing rules are given as the following (10L PCB):
      - VPROC1: 1 layer PWR+1 layer GND, 6 PTH Vias, S_1 length ≤ 450mil, S_1 width ≥ 200mil. (thickness ≥ 0.6mil)
      - VPROC2: 1 layer PWR+1 layer GND, 5 PTH Vias, S_1 length ≤ 450mil, S_1 width ≥ 200mil. (thickness ≥ 0.6mil)
      - VGPU: 1 layer PWR+1 layer GND, 6 PTH Vias, S_1 length ≤ 450mil, S_1 width ≥ 150mil. (thickness ≥ 0.6mil)
      - VCORE: 1 layer PWR+1 layer GND, 10 PTH Vias, S_1 length ≤ 450mil, S_1 width ≥ 150mil. (thickness ≥ 0.6mil)
      - VMODEM: 1 layer PWR+1 layer GND, 5 PTH vias, S_1 length ≤ 500mil; L_1 width ≥ 100mil. (thickness ≥ 0.6mil)
      - VSRAM_PROC1/VSRAM_PROC2/VSRAM_GPU/VSRAM_CORE:
        - 1 layer PWR+1 layer GND, 1 PTH Via, S_1 length ≤ 500mil, S_1 width ≥ 30mil. (thickness ≥ 0.6mil)
      - VEMI_VDD2:
        - SoC: Place at least 4 0201 caps right underneath AP with 3 PTH vias.
        - DRAM: Place at least 8 0201 caps close to VEMI_VDD2 balls.
      - VEMI_VDDQ:
        - SoC: Place at least 4 0201 caps right underneath AP with 3 PTH vias.
        - DRAM: Place at least 6 0201 caps close to VEMI_VDDQ balls.
   3) S_4 is defined as the power trace segment from "bottom cap" to AP. The corresponding PCB routing rules are given as the following:
      - Place 0201 and 0402 3-terminal SMD capacitors right beneath the power balls and connect the SMD capacitors with PTH/Laser via directly to reduce mounting inductance/resistance. S_4 should be routed as short as possible.

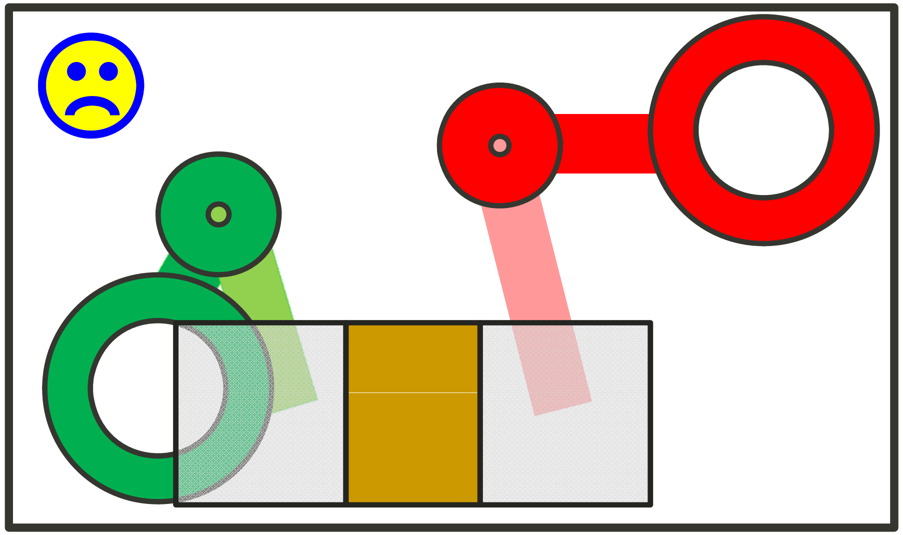
Mounting Inductance



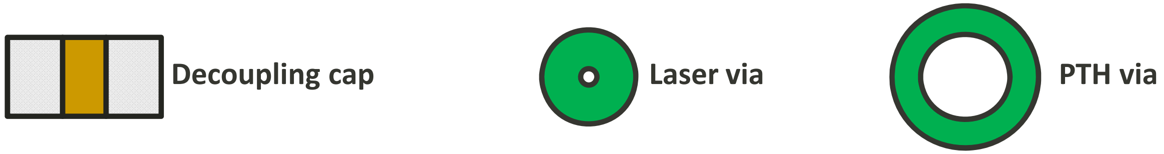
Via Interconnection



Good: Lowest mounting inductance



Bad: Excessive routing to increase inductance



● Design suggestions for via interconnection

Via interconnect is critical in delivering current between each layer and is usually the bottleneck in the entire PDN networking. Thus, we strongly recommend you follow the related PWR/GND layout guidelines.

1. Connect PWR/GND via to the "wide power trace" and place it as close to the decoupling capacitor as possible.
2. Each decoupling capacitor should have at last one pair PWR/GND via. If the routing space is available, more PWR/GND vias are recommended. Try distributing PTH and Laser vias uniformly and increase PTH via as much as you can.

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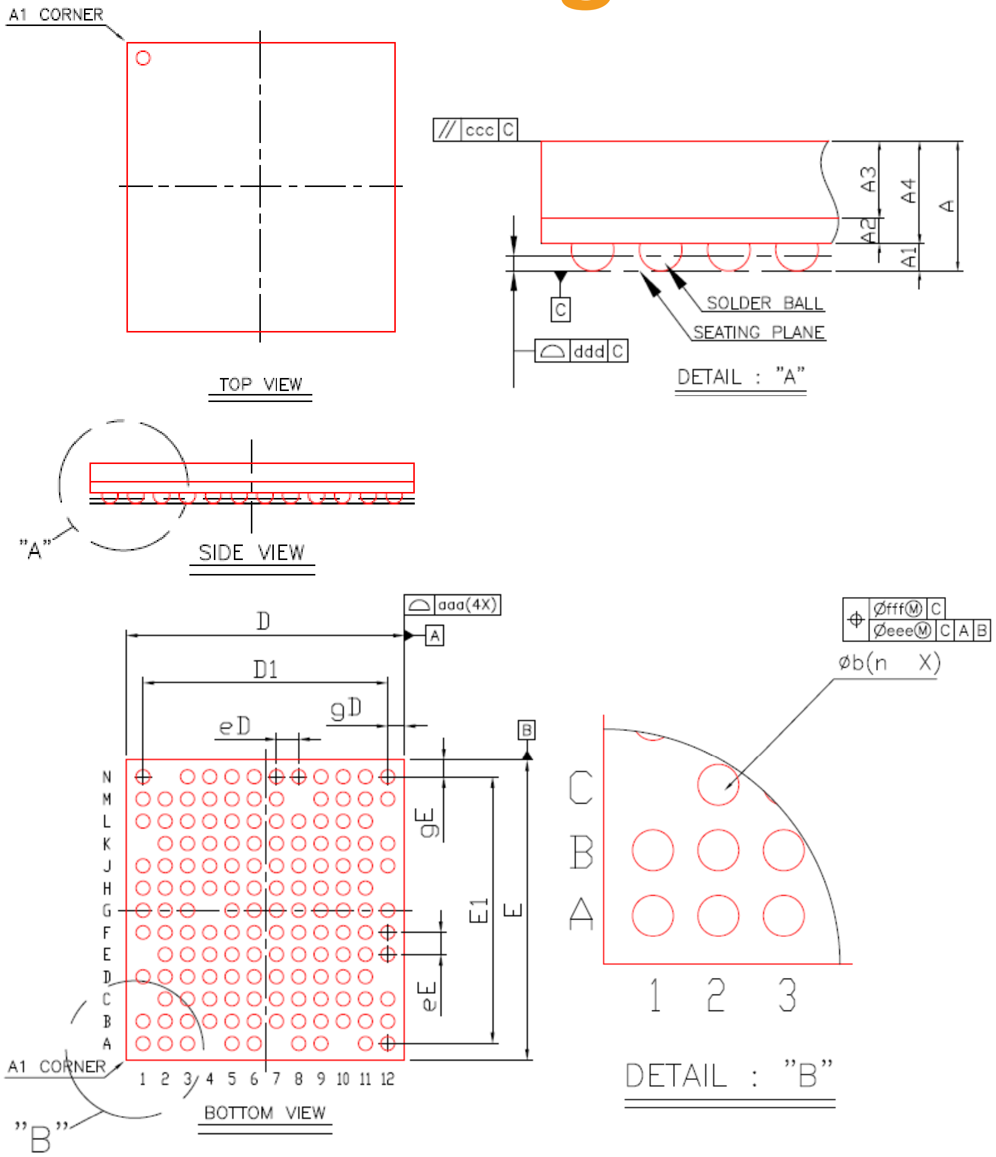
MT6177
PCB Layout Guideline

Package Outline of MT6177



Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MFC WFBGA		
Body Size	X	D	4.90	5.00	5.10
	Y	E	5.30	5.40	5.50
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.28 Ref.		
Substrate Thickness		A2	0.18 Ref.		
Substrate+Mold Thickness		A4	0.41	0.46	0.51
Total Thickness		A	–	–	0.70
Ball Diameter			0.25		
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	144		
Edge Ball Center to Center	X	D1	4.40		
	Y	E1	4.80		
Edge Ball Center to Package Edge	X	gD	0.300		
	Y	gE	0.300		

TITLE	PACKAGE OUTLINE		MEDIATEK	
	MFC WFBGA 144L 5.0 X 5.4 X 0.7mm			
DWG. NO.		REV.	SHEET	UNIT
MT-AP00502		A	1 OF 2	MM

MEDIATEK ADCT Connecting the Future

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MT6177 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	
A	DRX10	DRX7	DRX6		DRX2	DRX1		PRX13	PRX12		PRX9	PRX8	A
B	DRX9	DRX8	DRX5	DRX4	DRX3	LAAP1	GND	PRX14	PRX11	PRX10	PRX7	PRX6	B
C		DRX11	GND	GND	GND	GND	GND	GND	GND	GND	PRX5	PRX4	C
D	DRX13	DRX12	GND	GND	GND	GND	GND	GND	GND	GND	PRX3		D
E		DRX14	GND	GND	GND	VDD_RX LV	VDD_RX HV	GND	GND	GND	PRX2	PRX1	E
F	LAAD1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	F
G	TMEAS	GND	GND		GND	GND	GND	GND	GND	GND	TX_HB1	TX_UHB	G
H	RCAL	GND	GND	EN_BB	BSI_0_C K	GND	GND	GND	GND	GND	TX_HB2		H
J	XOI	VIO	GND	BSI_0_D 0	BSI_0_E N	GND	GND	GND	GND	TXO_GN D	TX_MB1	TX_MB2	J
K		GND	BSI_0_D 1	BSI_0_D 2	VDD_SX LV	GND	GND	GND	GND	TXO_GN D	TX_LB1	TX_MB3	K
L	DRX_BB _I1	DRX_BB _Q1	GND	GND	GND	GND	GND	GND	GND	TXO_GN D	TX_LB2		L
M	PRX_BB _Q1	GND	DRX_BB _Q0	PRX_BB _I0	DET_QP 0	DET_IN0	TXDET1		GND	TXO_GN D	TX_LB3	TX_LB4	M
N	PRX_BB _I1		DRX_BB _I0	PRX_BB _Q0	VDD_SX LF	DET_QN 0	DET_IP0	VDD_TX HV	TX_BB_ QN0	TX_BB_ QP0	TX_BB_I N0	TX_BB_I P0	N
	1	2	3	4	5	6	7	8	9	10	11	12	

RFDRX

RFPRX

26MHz Output

LTE BSI

RF TX

LTE PRXIQ

LTE DRXIQ

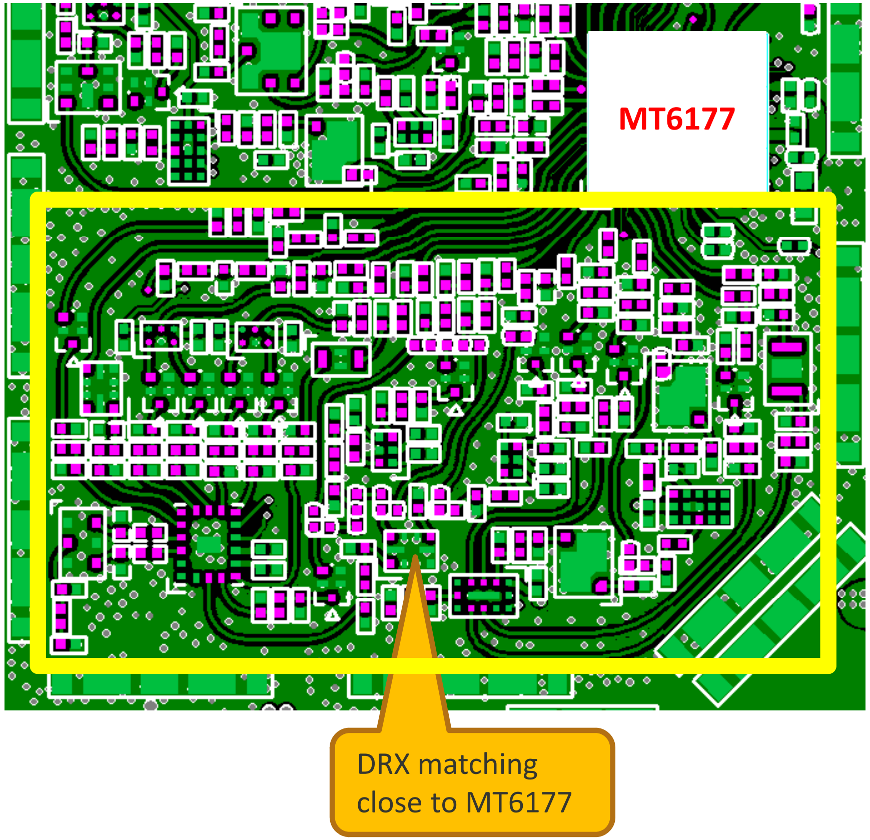
LTE TXIQ

MT6177 Placement (1/3)

- RF supports PRX (Primary RX) and DRX (Diversity RX). MT6177 has two receiver circuits.
- DRX matching components should be placed near MT6177.

MT6177 DRX

IC ball number	IC ball name	PCB net name
DRX1	A6	RF_B12B17_DRX_RFIC
DRX2	A5	RF_B8_DRX_RFIC
DRX3	B5	RF_B20_DRX_RFIC
DRX4	B4	RF_B5B26B27_DRX_RFIC
DRX5	B3	RF_B28_DRX_RFIC
DRX6	A3	RF_B39_DRX_RFIC
DRX7	A2	RF_B3_DRX_RFIC
DRX8	B2	RF_B2_DRX_RFIC
DRX9	B1	RF_B32_DRX_RFIC
DRX10	A1	RF_B1B4_DRX_RFIC
DRX11	C2	RF_B40_DRX_RFIC
DRX12	D2	RF_B38B41_DRX_RFIC
DRX13	D1	RF_B7_DRX_RFIC
DRX14	E2	RF_B42_DRX_RFIC

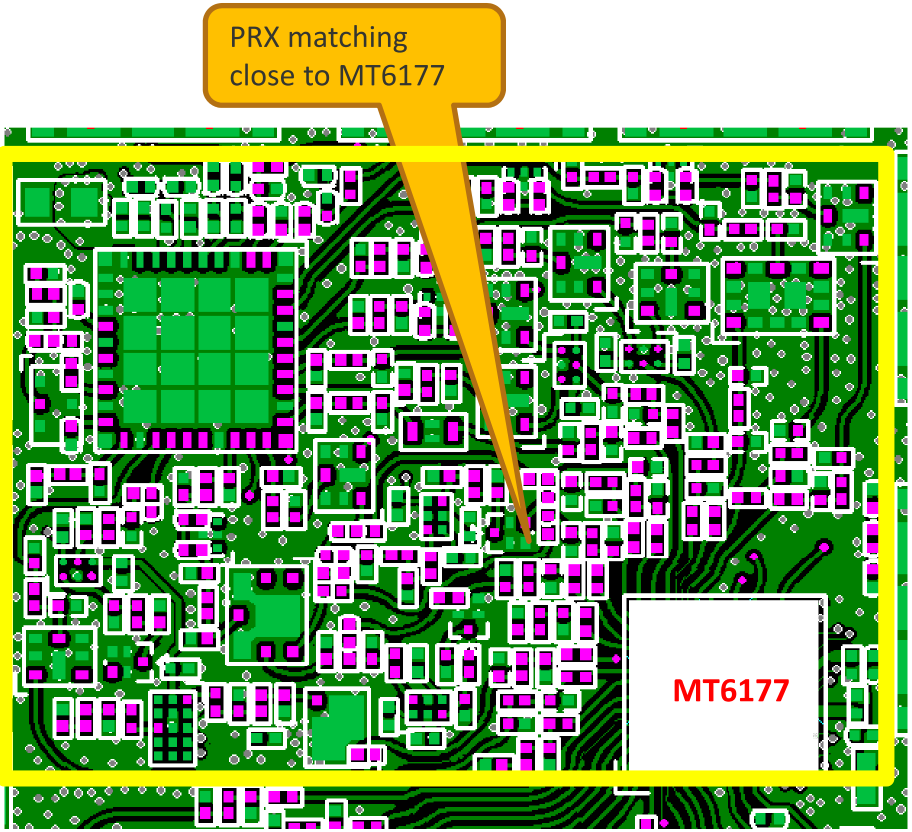


MT6177 Placement (2/3)

- PRX matching components should be placed near MT6177.

MT6177 PRX

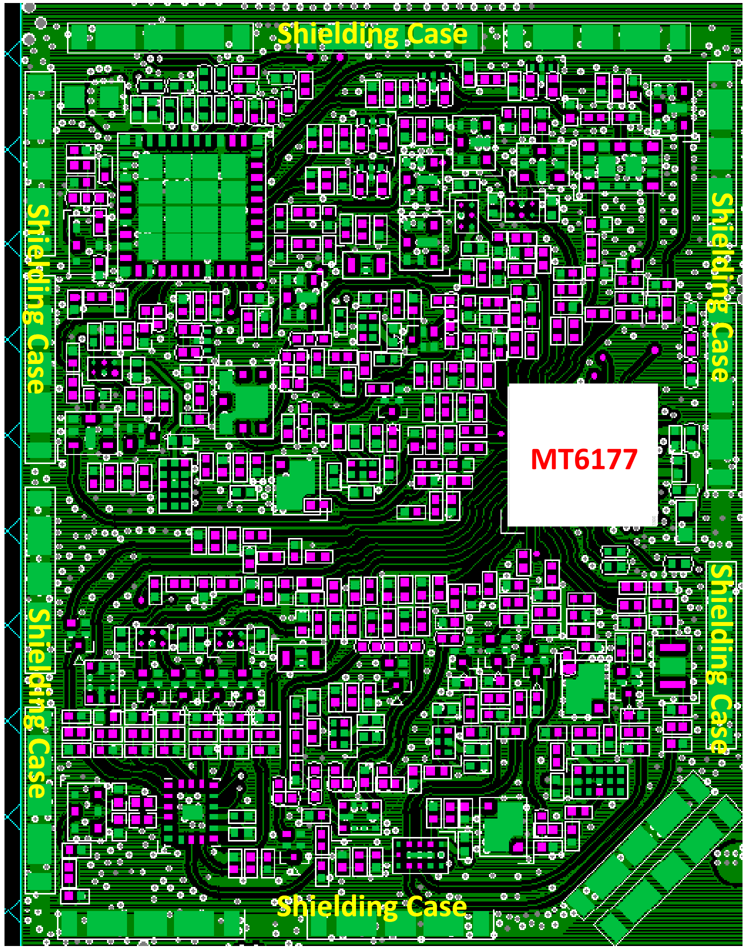
IC ball number	IC ball name	PCB net name
PRX1	E12	RF_B12B17_PRX_RFIC
PRX2	E11	RF_B8_PRX_RFIC
PRX3	D11	RF_B20_PRX_RFIC
PRX4	C12	RF_B5B26B27_PRX_RFIC
PRX5	C11	RF_B28_PRX_RFIC
PRX6	B12	RF_B34B39_PRX_RFIC
PRX7	B11	RF_B3_PRX_RFIC
PRX8	A12	RF_B2_PRX_RFIC
PRX9	A11	RF_B32_PRX_RFIC
PRX10	B10	RF_B1B4_PRX_RFIC
PRX11	B9	RF_B40_PRX_RFIC
PRX12	A9	RF_B38B41_PRX_RFIC
PRX13	A8	RF_B7_PRX_RFIC
PRX14	B8	RF_B42_PRX_RFIC



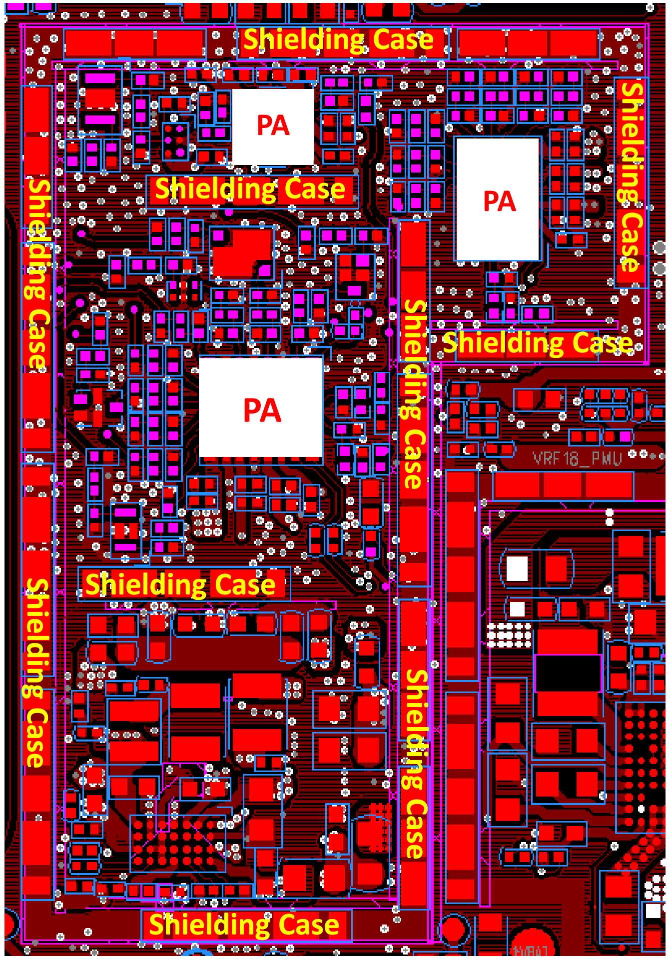
MT6177 Placement (3/3)

- MT6177 and PA IC should have their own shielding case to prevent de-sense issues.

Top side



Bottom side

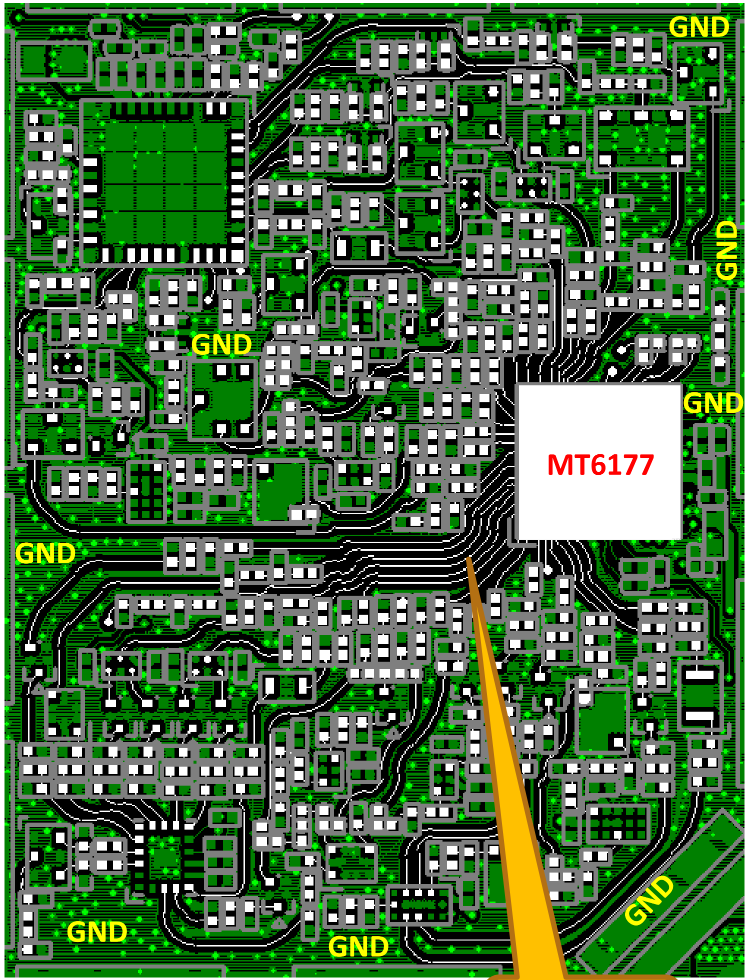


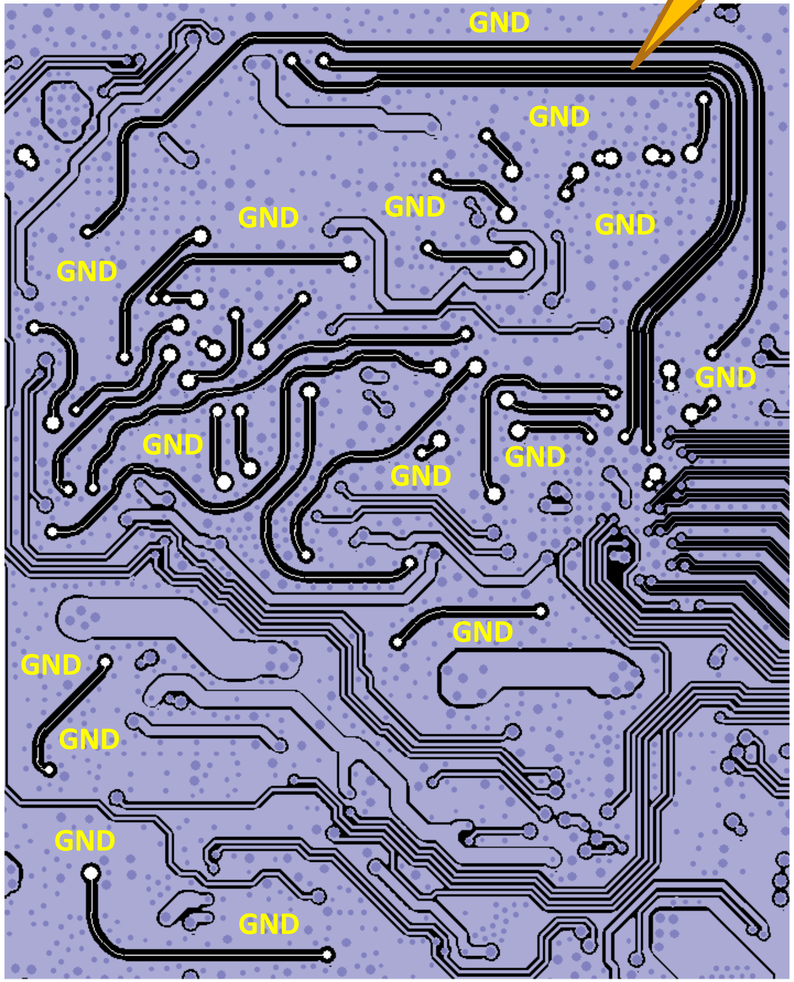
CONFIDENTIAL B

MT6177 TX/RX Signals

- Impedance control is necessary for all RF signals.
- Make sure that the routing impedance is single-ended 50Ω for TX/PDET/RX.

Impedance 50Ω

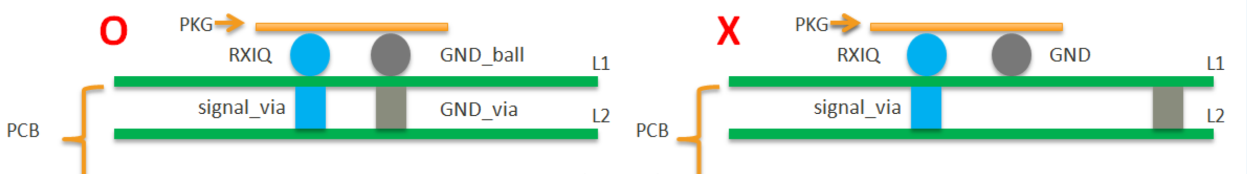




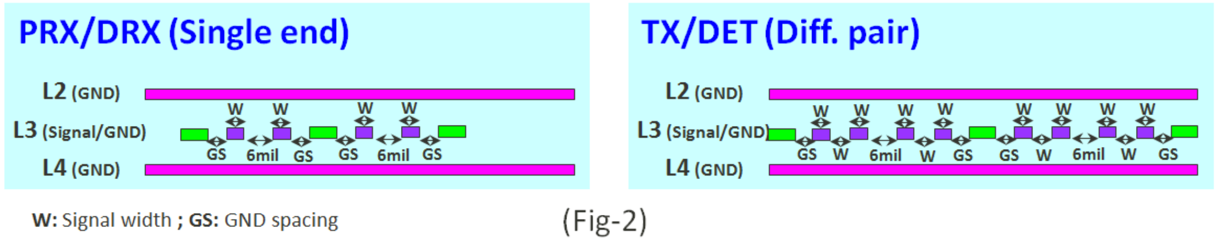
Impedance 50Ω

MT6177 IQ Signals (1/3)

a. All GND ball adjacent RXIQ must be well connected @ L1. (Fig-1)
b. The RXIQ signal must have GND via close to its layer transition. (Fig-1)
c. All RXIQ signals should have GND shielding by group (adjacent up/down layers). (Fig-2)
d. All TXIQ, RXIQ, DETIQ layout length must < 20mm to prevent bad isolation.



(Fig-1)



(Fig-2)

IC ball name	IC ball number
DET_IN0	M6
DET_IP0	N7
DET_QN0	N6
DET_QP0	M5
DRX_BB_I0	N3
DRX_BB_I1	L1
DRX_BB_Q0	M3
DRX_BB_Q1	L2
PRX_BB_I0	M4
PRX_BB_I1	N1
PRX_BB_Q0	N4
PRX_BB_Q1	M1
TX_BB_IN0	N11
TX_BB_IP0	N12
TX_BB_QN0	N9
TX_BB_QP0	N10

MT6177 IQ

MT6177 IQ Signals (2/3)

Layout not recommended

Figure 1 shows the ABB IQ are routed beneath the PMIC power nets even with ground plane shielding.

But the magnetic coupling from PMIC switching node could cause de-sense issue.

Layout recommended

Figure 2 shows the ABB IQ are routed away from PMIC power nets to avoid de-sense issue.

No overlap between PMIC nets and ABB IQ region.

Not Recommended

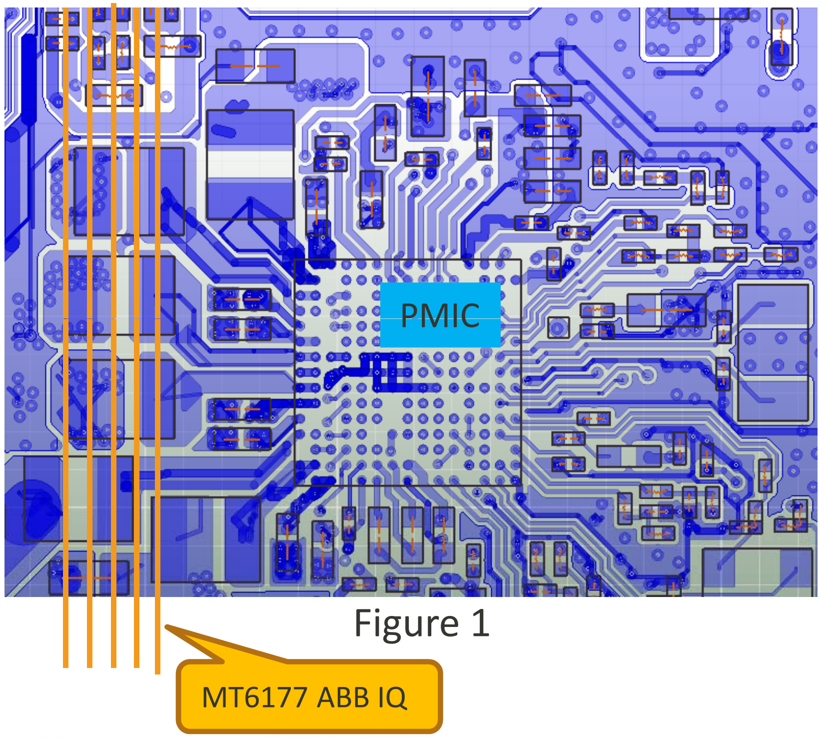


Figure 1

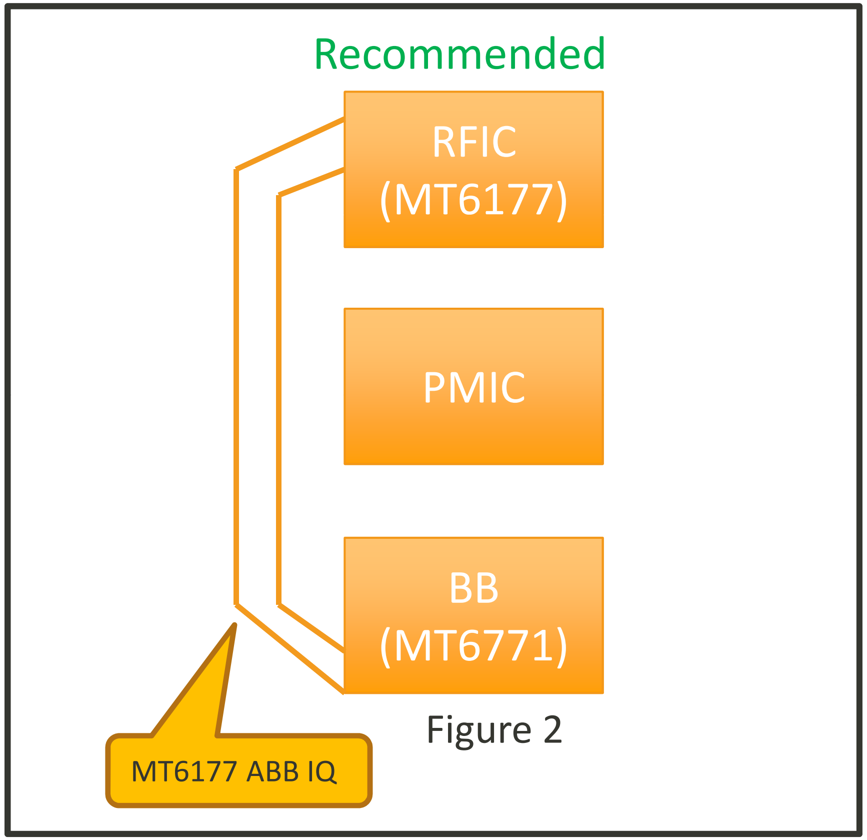


Figure 2

MEDIATEK ADCT Connecting the Future

MT6177 IQ Signals (3/3)

Layout not recommended

Figure 1 shows the PMIC power nets via are routed in the ABB IQ region in the PCB inner layer even with ground shielding

But the low frequency PMIC switching noise could couple to RX IQ and cause de-sense issue.

Not Recommended

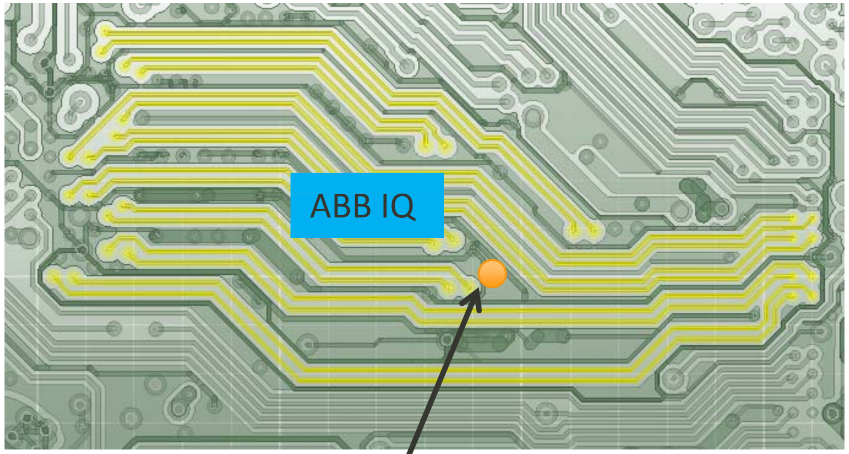


Figure 1

PMIC power nets

Layout recommended

Figure 2 shows PMIC power nets via are away from ABB IQ region at least 25mil to avoid de-sense issue.

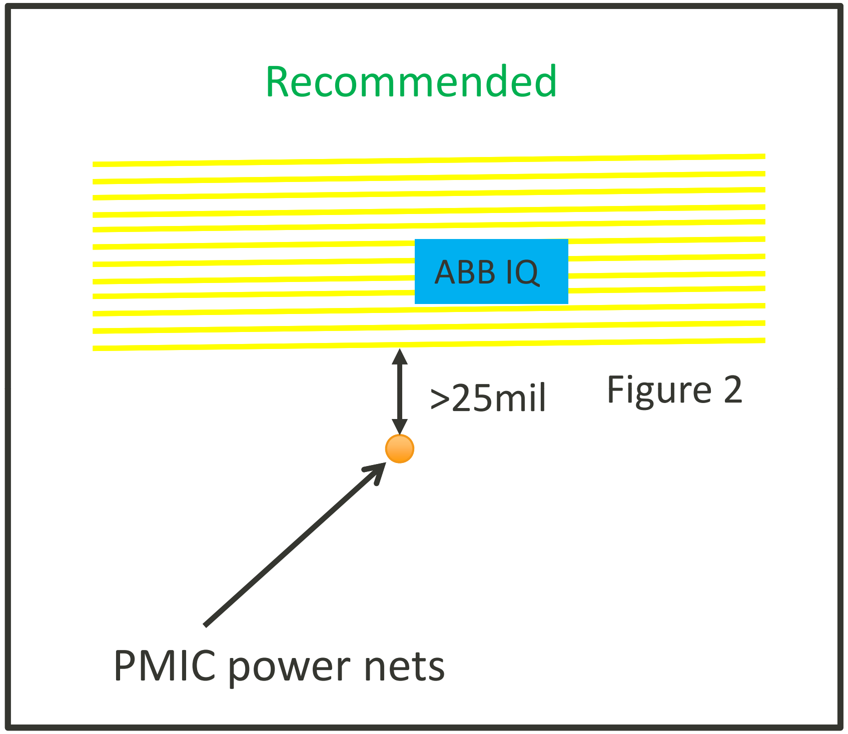


Figure 2

MT6177 Duplexer

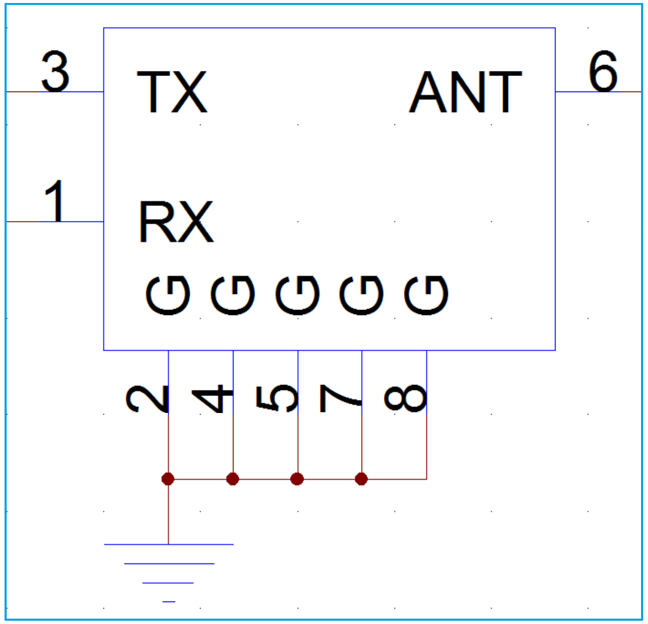
- **Duplexer notice**

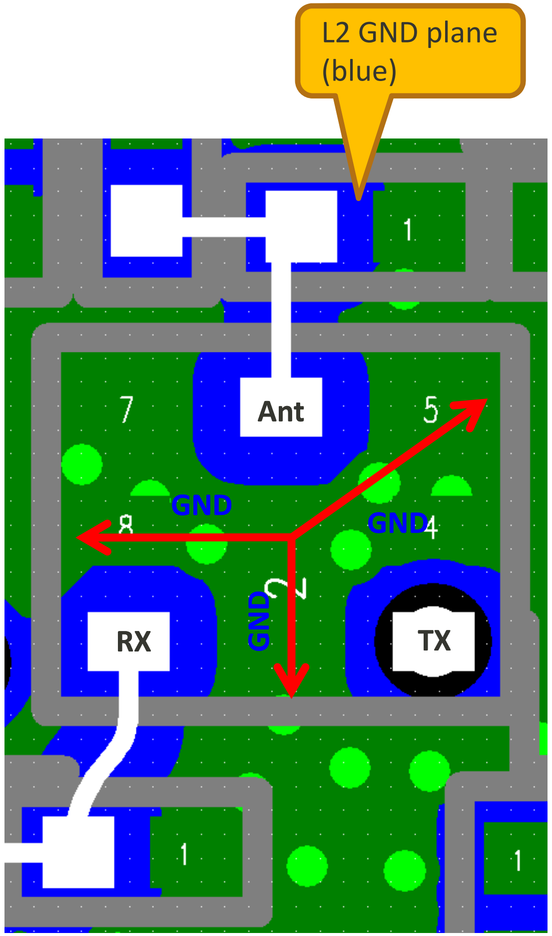
a. Enlarge L1 copper pouring range for duplexer GND pins (2, 4, 5, 7, 8).

b. Avoid parallel routing between ANT/RX/TX signals.

c. Maintain good isolation between ANT/RX/TX by:
   1. GND shielding between these three paths.
   2. Good grounding with plenty of GND via.

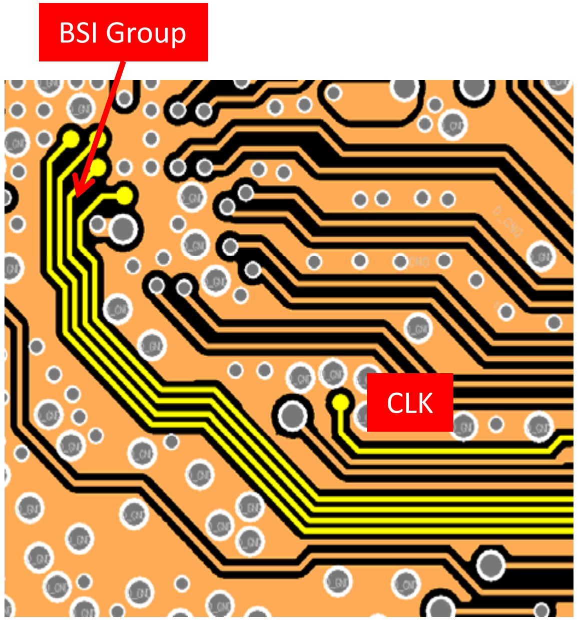
d. There should be good GND plane at L2 for reference.





Others for MT6177

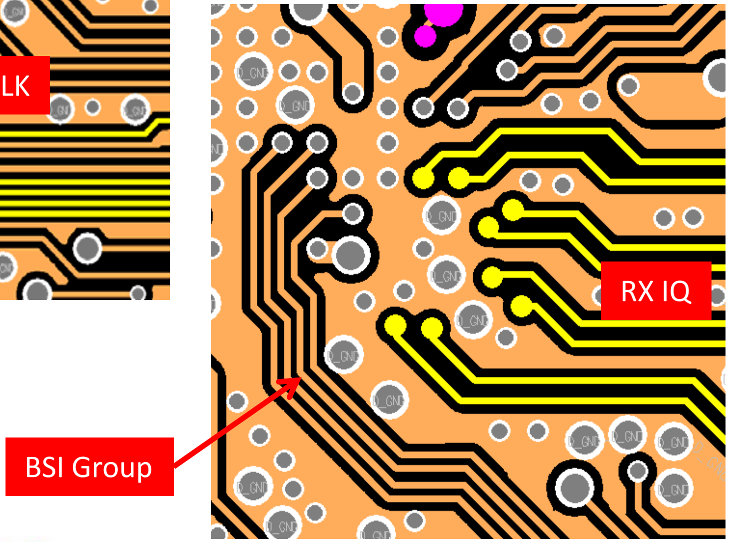
a. CLK signal should have GND shielding and avoid routing this net between BSI signals. (Fig-1)
b. BSI signals should have GND shielding by group (adjacent up/down layers). (Fig-1)
c. Must have ground via close to the RXIQ when layer change happens. (Fig-2)
d. RFFE MIPI signal (MIPI0_SCLK , MIPI0_SDATA) should be as far as possible from RF signals. (Fig-3)



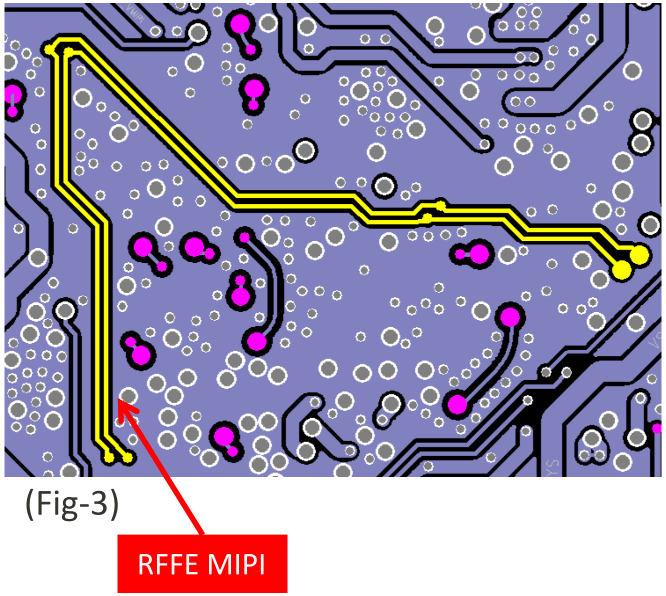
(Fig-1)

MT6177 BSI

IC ball name	IC ball number
BSI_0_CK	H5
BSI_0_D0	J4
BSI_0_D1	K3
BSI_0_EN	J5



(Fig-2)



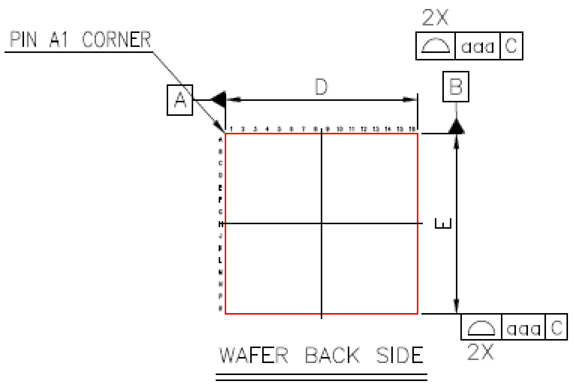
(Fig-3)

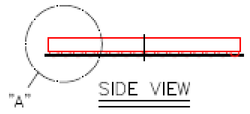
Outlines

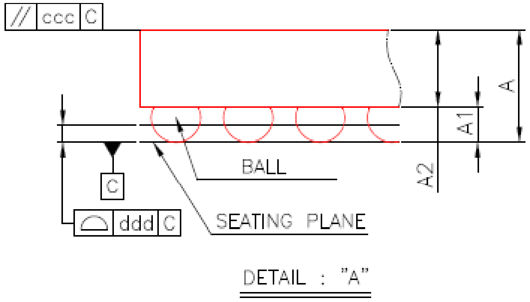
- Packaging
  - Package outline of MT6771
  - MT6771 footprint recommendation
  - MT6771 ball out design
- General Guidelines
  - PCB stack-up recommendation
  - Placement notes
- Design Guidelines for High-Speed Digital Signals
  - LPDDR4X/LPDDR3
  - PDN design
- Others
  - MT6177 (RF transceiver)
  - MT6358 (PMU)
  - MT6631 (BT/FM/Wi-Fi/GPS)
  - MT6370 (Battery Charger/USB_PD)
  - eMMC/USB/MIPI/SIM Card/T-Card

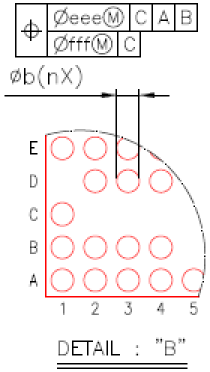
MT6358
PCB Layout Guideline

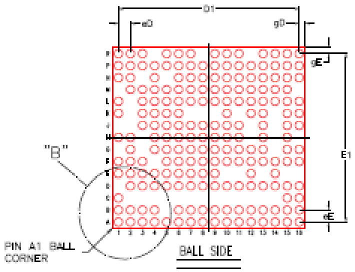
Package Outline of MT6358











Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MIFO WLCSP		
Body Size	X	D	6.30	6.40	6.50
	Y	E	5.90	6.00	6.10
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Total Thickness		A	0.580	0.620	0.660
Ball Stand Off		A1	0.170	0.195	0.220
Body Thickness		A2	0.400	0.425	0.450
Ball Width		b	0.245	0.275	0.305
Ball Diameter			0.250		
Body Edge Tolerance		aaa	0.10		
Body Flatness		ccc	0.10		
Coplanarity		ddd	0.05		
Ball Offset (Package)		eee	0.10		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	194		
Edge Ball Center to Center	X	D1	6.00		
	Y	E1	5.60		
Edge Ball Center to Body Edge	X	gD	0.20		
	Y	gE	0.20		

MT6358 Ball Map

194	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NC	VS1	GND_VS1	VPA	VSYS_VPA	VSYS_VPROC11	VPROC11	GND_VPROC11	VPROC12	VSYS_VPROC12	VSYS_VGPU	VGPU	GND_VCORE	VCORE	VSYS_VCORE	NC	A
B	VSYS_VS1	VS1	GND_VS1	GND_VPA		VSYS_VPROC11	VPROC11	GND_VPROC11	VPROC12	VSYS_VPROC12	VSYS_VGPU	VGPU	GND_VCORE	VCORE	VSYS_VCORE	GND_VCORE_FB	B
C	VSYS_VS1														GND_VGPU_FB	VCORE_FB	C
D		PWRKEY	EXT_PMIC_EN1	RESETB	VPA_FB	VPROC11_FB	GND_VPROC11_FB	GND_VPROC12	GND_VPROC12	GND_VPROC12_FB	VDRAM1_FB	GND_VGPU	GND_VGPU	VGPU_FB	VMODEM_FB	VS2_FB	D
E	GND_SMPS	VSYS_SMPS	VEFUSE	VS1_LDO1	EXT_PMIC_EN2	VCAMIO	VS1_FB	PMU_TESTMODE	VPROC12_FB			GND_VDRAM1_FB		GND_VMODEM_FB			E
F	AU_V18N	FLYN	VIO18		VRF18	VCN18	D_GND	D_GND	D_GND	RTC32K_1V8_0	SPI_CLK	WDTRST_B_IN	SPI_CSN	VSYS_VMODEM	VMODEM	VMODEM	F
G		FLYP		AU_HPR	AU_LOLP	AU_LOLN	D_GND	D_GND	D_GND	SPI_MISO	SPI_MOSI	RTC32K_1V8_1	HOMEKEY		GND_VMODEM	GND_VMODEM	G
H	AVSS18_AUD	AVDD18_AUD		AU_HPL	AU_REFN	AU_HSN	D_GND	D_GND	D_GND	AUD_CLK_MISO	AUD_DAT_MISO1		SCP_VREQ_VAO		GND_VDRAM1		H
J			AVDD28_AUD	HP_EINT	AVSS28_AUD	AU_HSP	SRCLKEN_IN1	DVDD18_DIG	AUD_DAT_MOSI0	AUD_SYNC_MISO	AUD_DAT_MISO0		SD_CARD_DET_N		VDRAM1	VSYS_VDRAM1	J
K	AU_VIN0_P		AU_VIN2_N	AU_VIN2_P	AU_MICBIAS0	ACCDET				AUD_SYNC_MOSI		VCDT	CHRLDO		VSYS_VS2	VSYS_VS2	K
L	AU_VIN0_N		AU_VIN1_N	AU_VIN1_P	AU_MICBIAS1	FSOURCE	SRCLKEN_IN0	DVSS18_IO	DVDD18_IO	AUD_DAT_MOSI1	AUD_CLK_MOSI	BATON	BATADC	GND_VS2	VS2	VS2	L
M		AUXADC_VIN	AVDD18_AUXADC	AVSS18_AUXADC	CS_N	VAUX18	RTC32K_2V8	VRTC28	VBIF28	VCAMA1	VSYSSNS	VREF	UVLO_VTH	VS2_LDO4	VCAMD		M
N	XTAL1	AVSS22_XO_ISO		XO_NFC		CS_P	VSIM1	VUSB	VIO28	VCAMA2	VSYS_LDO3	VCN33	GND_VREF	VS2_LDO2	VRF12	VA12	N
P	XTAL2	AVSS22_XO	XO_WCN	XO_SOC	XO_EXT	VXO22	VSYS_LDO1	VLDO28	VSYS_LDO2	VSIM2	VIBR	VSRAM_PROC11	VS2_LDO3	VSRAM_OTHERS	VDRAM2	VRF12_S	P
R	NC	AVSS22_XOBUF	XO_CEL		VAUD28	VCAMA1	VFE28		VMC	VMCH	VEMC		VSRAM_PROC12	VSRAM_GPU	VS2_LDO1	NC	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Color	Legend
Green	Power Input
Purple	Buck Output
Orange	LDO Input
Pink	LDO Output
Gray	GND
Cyan	Audio Input/Output
Blue	AUX_ADC
Dark purple	DCXO
Magenta	RTC
Red	Charge

MT6358 Power Input (1/2)

VSYS Input

- VSYS 22uF capacitor is placed near MT6358 **VSYS** input balls (Fig. 2).
- Routing from 22uF VSYS capacitor uses start topology to connect to each device.

  1. **VSYS** input for BUCK. (Fig. 3)

  2. **VSYS** input for LDO. (Fig. 3)
- Follow the trace width rule in Fig. 4.
- All the decoupling capacitors should be placed near MT6358. The priority is buck capacitor then decoupling capacitor of LDO. (Fig.1)

Fig. 4

IC Ball Name	IMAX(mA)
VSYS_SMPS	10
VSYS_VPROC11	3600
VSYS_VPROC12	2700
VSYS_VCORE	3600
VSYS_VMODEM	1500
VSYS_VS1	2000
VSYS_VS2	1500
VSYS_VPA	1750
VSYS_GPU	2000
VSYS_VDRAM1	1500
VSYS_LDO1	2000
VSYS_LDO2	2000
VSYS_LDO3	2000

Fig. 1

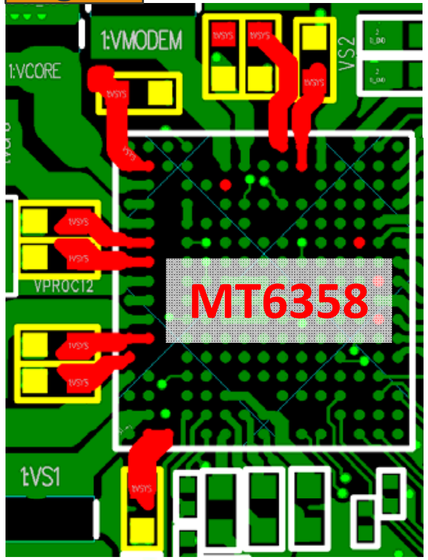


Fig. 2

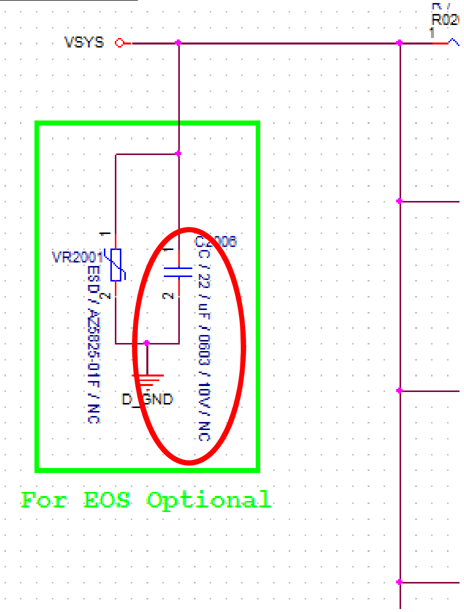
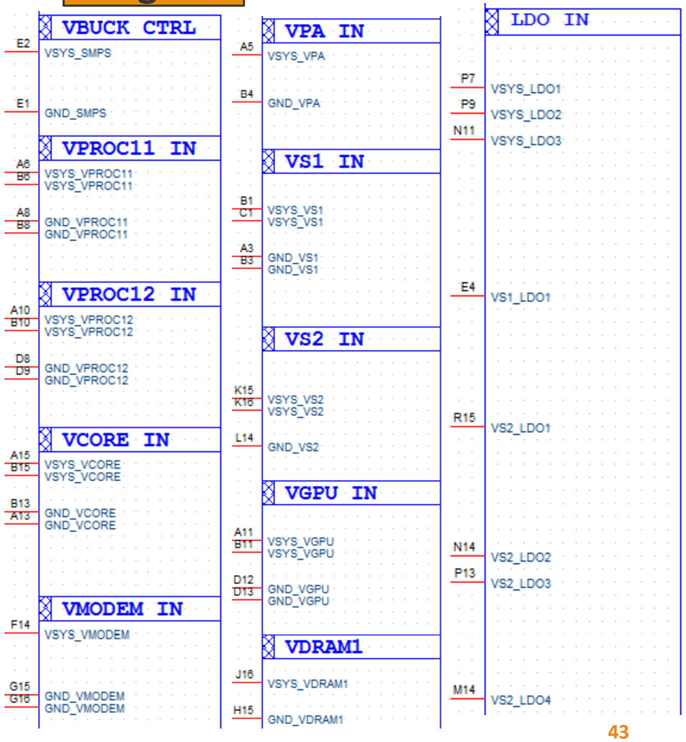


Fig. 3



MT6358 Power Input (2/2)

- **Layout method of MT6358 power Input for Buck GND**
  - Buck GND balls are connected to buck capacitors close to pin with plane or trace (Trace Width > **8mil * N (ball number) + M (ball pitch)**). (Fig.1~2)
  - Buck GND balls should be connected to buck capacitors first and isolated from the nearby GND trace and plane then connected to main GND at L3 (Fig.1~2).

Fig.1

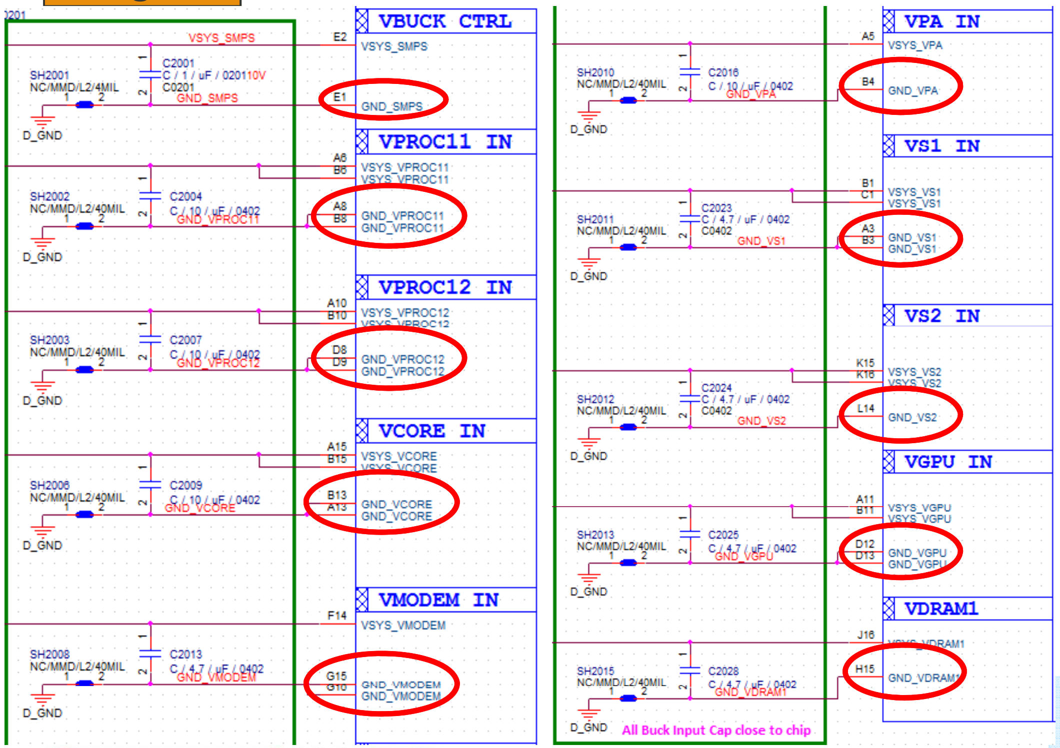
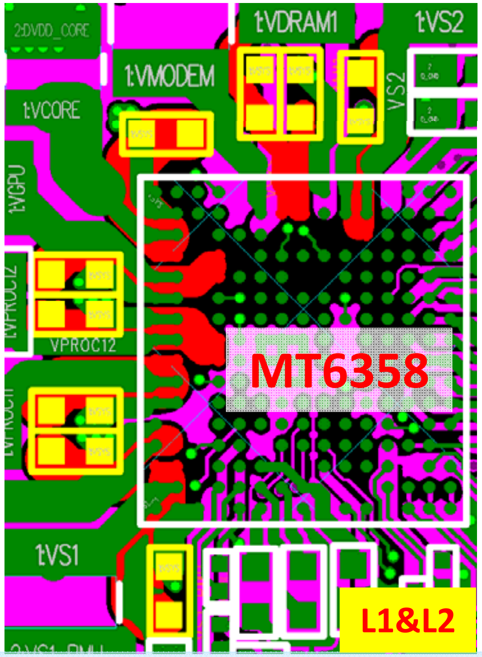


Fig.2



Layer 2: BUCK GND is isolated from nearby GND trace and plane.

MT6358 Buck Output (1/2)

- The buck inductors should be placed near MT6358. (Fig.1)
- The output current is shown in Fig.2.

Fig.1

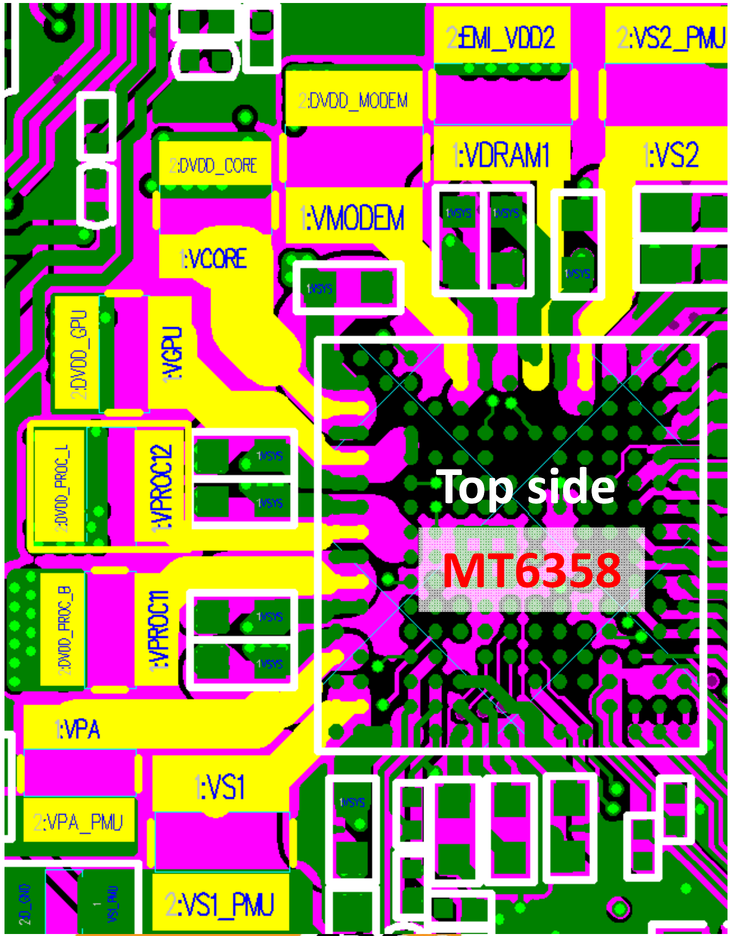
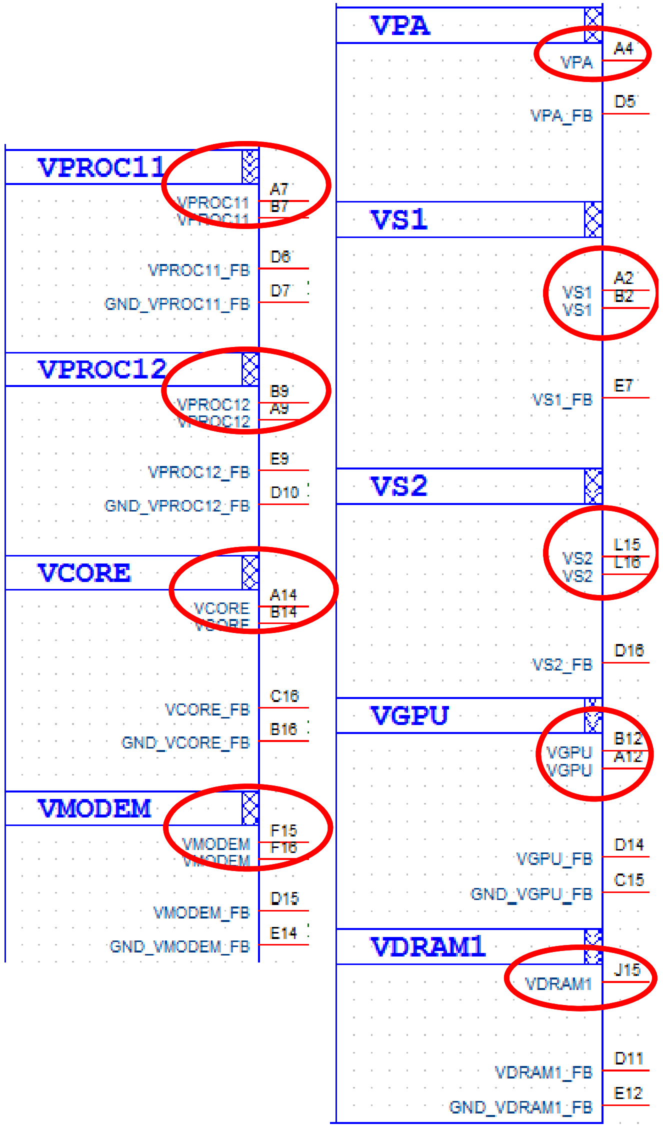


Fig.2

Output ball name	Output Current(mA)
VS1	2000
VS2	2000
VDRAM1	2000
VMODEM	2000
VPA	1000
VPROC11	5000
VPROC12	3190
VCORE	5000
VGPU	3310



CONFIDENTIAL B

MT6358 Buck Output (2/2)

- Those signals are differential pairs and should be shielded by GND and far away from noise signals (Fig.1 ~ Fig.2).
  1. VMODEM_FB/GND_VMODEM_FB
  2. VPROC11_FB/GND_VPROC11_FB
  3. VPROC12_FB/GND_VPROC12_FB
  4. VCORE_FB/GND_VCORE_FB
  5. VGPU_FB/GND_VGPU_FB
  6. VDRAM1_FB/GND_VDRAM1_FB
  7. VS1_FB, VS2_FB, VPA_FB

Fig. 1

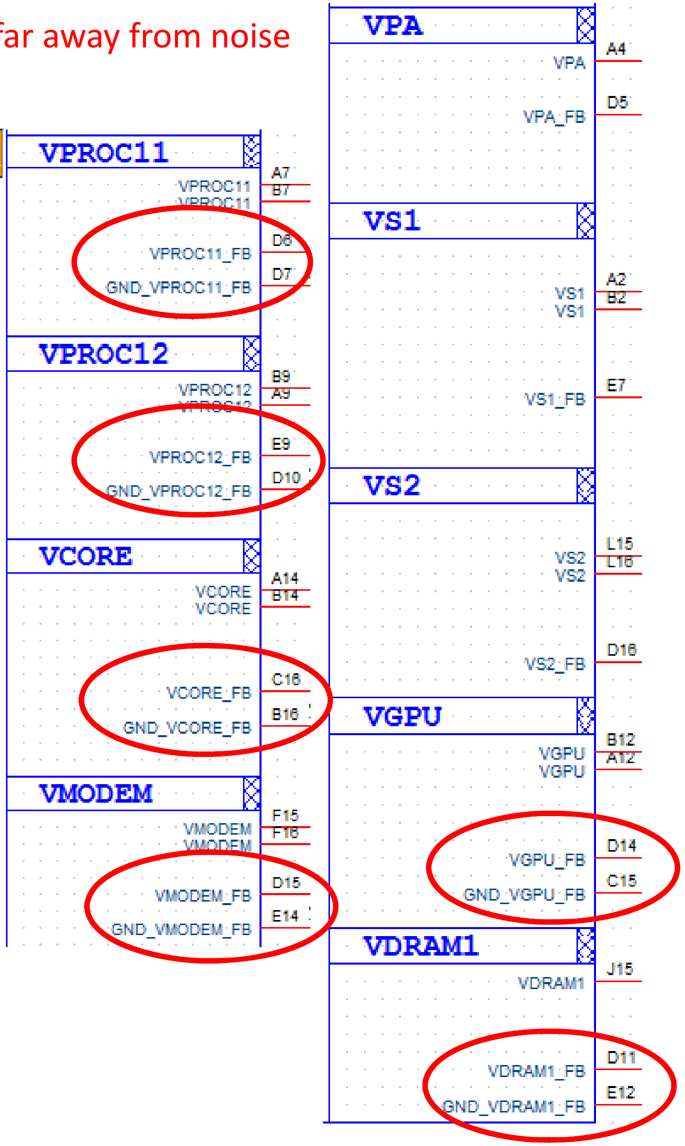
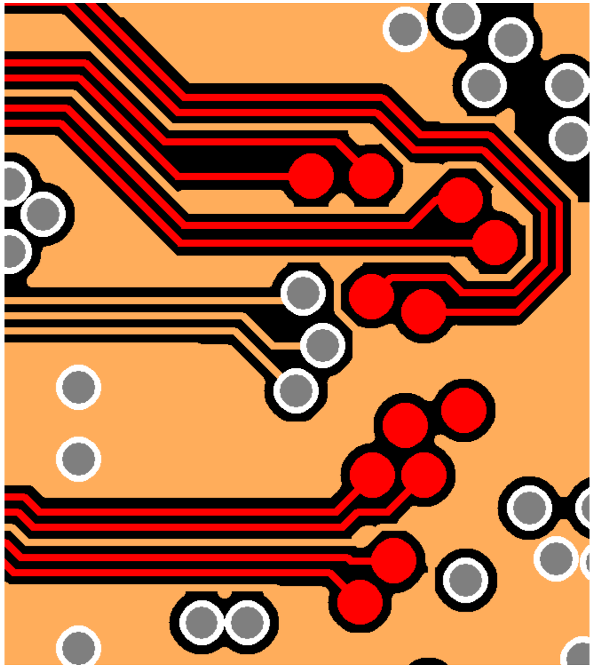
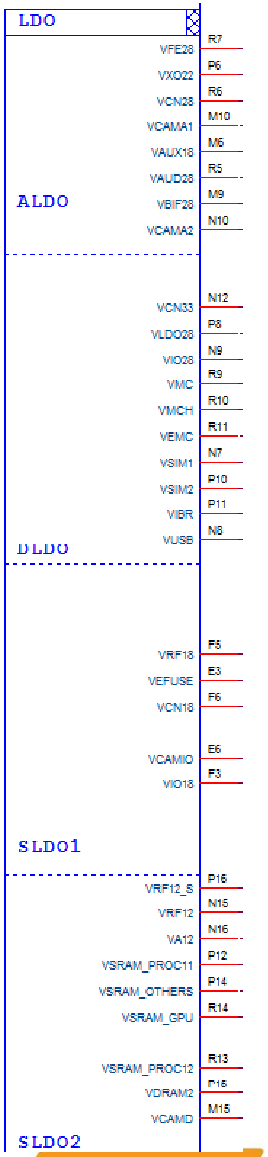


Fig. 2



MT6358 LDO Output (1/2)

- See table. for the suggested LDO output layout.

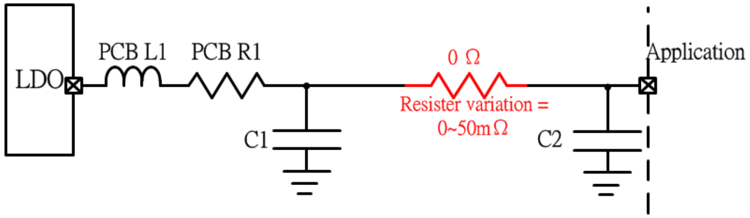


1. Trace width≧6mil
2. Value and placement of Capacitor please refer design notice

Ball name	Imax	Trace Length	Trace Width	Rpcb H=50um, 1/3 oz	PCB drop voltage
VFE28	50mA	2500mil	6mil	670mΩ	34mV
VXO22	25mA	2500mil	6mil	670mΩ	17mV
VCN28	50mA	2500mil	6mil	670mΩ	34mV
VCAMA1	200mA	2500mil	6mil	670mΩ	134mV
VAUX18	50mA	2500mil	6mil	670mΩ	34mV
VAUD28	50mA	2500mil	6mil	670mΩ	34mV
VBIF28	50mA	2500mil	6mil	670mΩ	34mV
VCAMA2	200mA	2500mil	6mil	670mΩ	134mV
VCN33	800mA	1000mil	20mil	80mΩ	64mV
VLDO28	400mA	2500mil	10mil	402mΩ	161mV
VIO28	200mA	2500mil	6mil	670mΩ	134mV
VMC	200mA	2500mil	6mil	670mΩ	134mV
VMCH	800mA	1000mil	20mil	80mΩ	64mV
VEMC	800mA	1000mil	20mil	80mΩ	64mV
VSIM1	200mA	2500mil	6mil	670mΩ	134mV
VSIM2	200mA	2500mil	6mil	670mΩ	134mV
VIBR	200mA	2500mil	6mil	670mΩ	134mV
VUSB	200mA	2500mil	6mil	670mΩ	134mV
VRF18	450mA	1000mil	14mil	115mΩ	52mV
VEFUSE	300mA	2500mil	8mil	503mΩ	151mV
VCN18	300mA	2500mil	8mil	503mΩ	151mV
VCAMIO	300mA	2500mil	8mil	503mΩ	151mV
VIO18	600mA	1000mil	16mil	101mΩ	60mV
VRF12_S	0mA	x	x	x	x
VRF12	800mA	1000mil	20mil	80mΩ	64mV
VA12	300mA	2500mil	8mil	503mΩ	151mV
VSRAM_PROC11	600mA	1000mil	16mil	101mΩ	60mV
VSRAM_OTHERS	600mA	1000mil	16mil	101mΩ	60mV
VSRAM_GPU	600mA	1000mil	16mil	101mΩ	60mV
VSRAM_PROC12	600mA	1000mil	16mil	101mΩ	60mV
VDRAM2	600mA	1000mil	16mil	101mΩ	60mV
VCAMD	600mA	2500mil	16mil	251mΩ	151mV

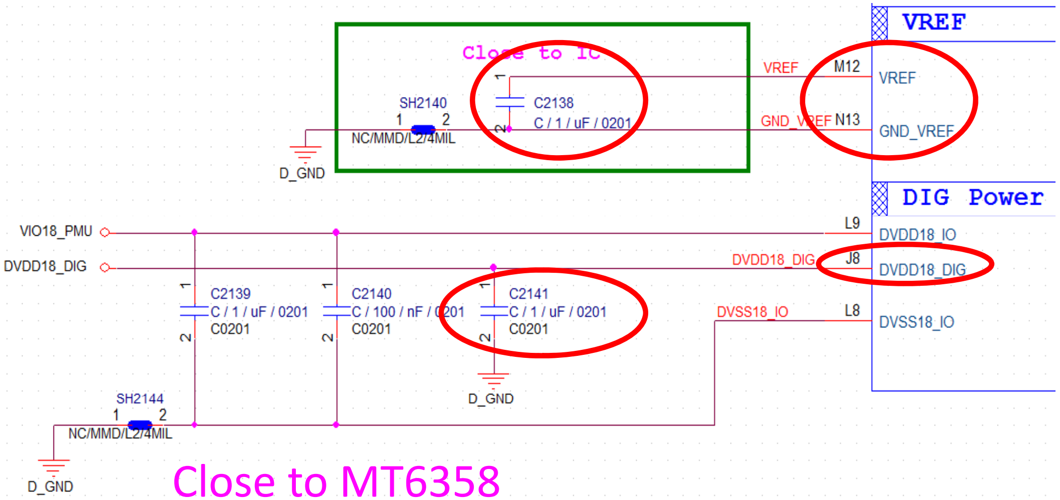
- VRF18/VRF12/VRF12_S:
  - **Traces should be in inner layer or under shielding case.**
- VRF12_S:
  - **For MT6177, VRF12_S should connect to ball VRF12**
  - **For MT6185M, VRF12_S should connect to VRF12 output capacitor**
- Trace width/length can adjust by application Imax

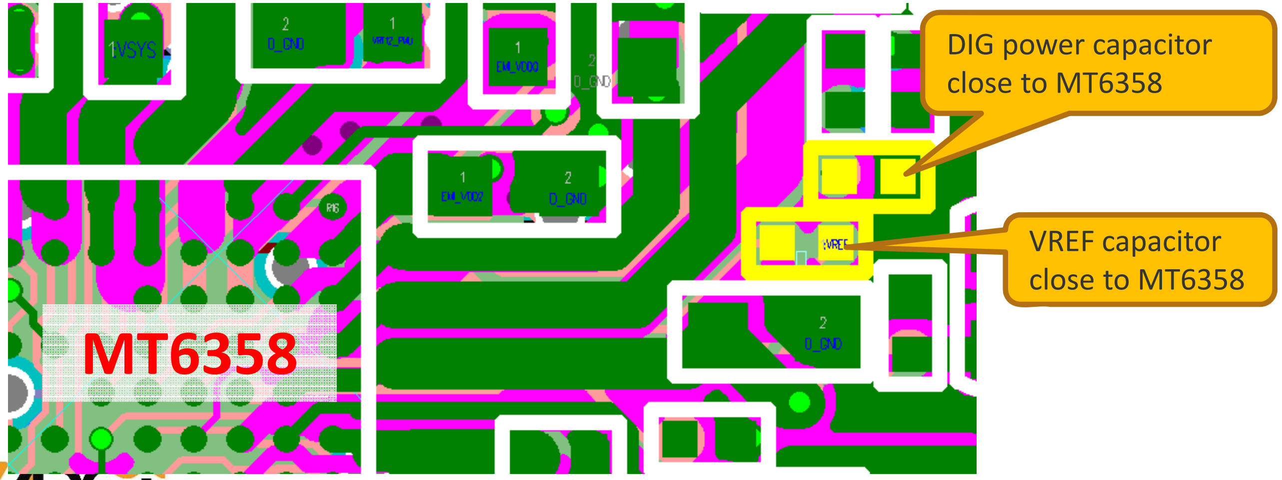
If trace is series 0Ω resister, 0Ω resister is having 0~50mΩ variation. It would be drop voltage.



MT6358 LDO Output (2/2)

- VREF capacitor should be placed near M12/N13 pin.
- DVDD18_DIG capacitor should be placed near J8 pin.





MT6358 Audio (1/3)

- The signals in Table 1 should be routed as differential pairs and shielded by GND (adjacent and up/down layers) and trace width ≧ 4mil. (HSP/HSN trace width ≧ 6mil)
- AU_HPR/AU_HPL signals should be shielded by GND respectively and trace width ≧ 6mil.
- Other signals should be routed orthogonally to other signals between adjacent layers.
- Related capacitors should be placed near MT6358. (Fig. 1 ~ Fig. 4)

Fig.1

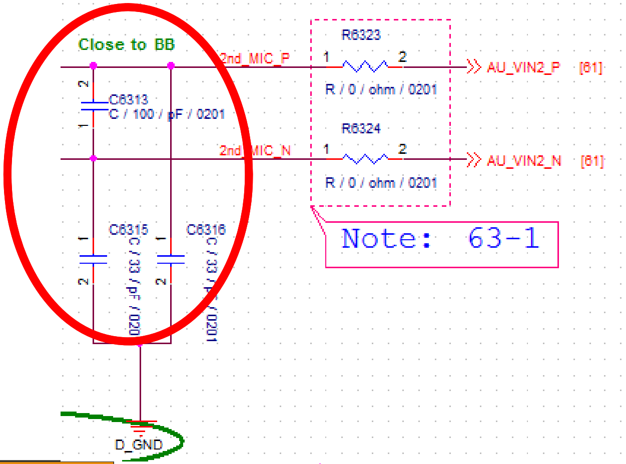


Fig.2

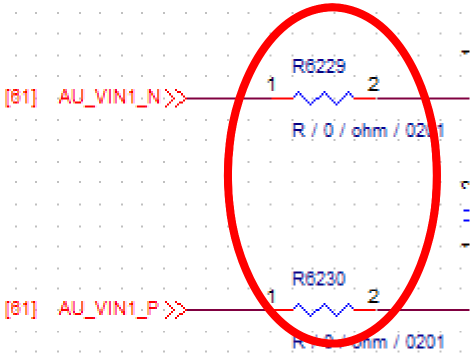


Fig.3

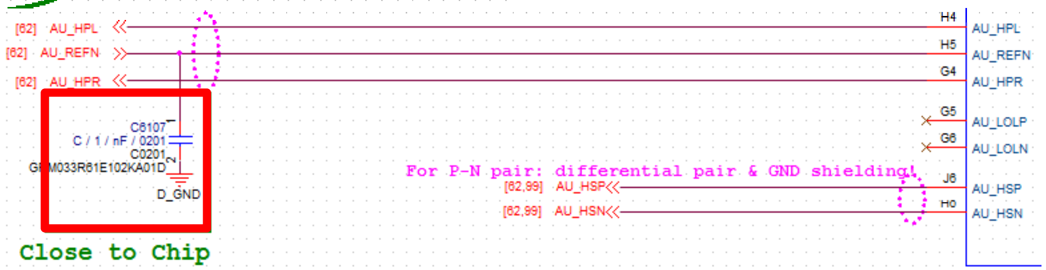
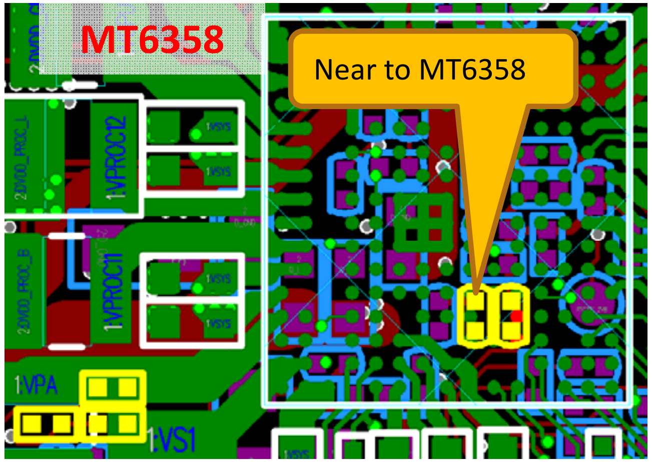


Table 1

Ball number	PCB net name	IC ball name
K1	AU_VIN0_P	AU_VIN0_P
L1	AU_VIN0_N	AU_VIN0_N
L4	AU_VIN1_P	AU_VIN1_P
L3	AU_VIN1_N	AU_VIN1_N
K4	AU_VIN2_P	AU_VIN2_P
K3	AU_VIN2_N	AU_VIN2_N
H6	AU_HSN	AU_HSN
J6	AU_HSP	AU_HSP
G4	**AU_HPR**	**AU_HPR**
H4	**AU_HPL**	**AU_HPL**
G5	**AU_LOLP**	**AU_LOLP**
G6	**AU_LOLN**	**AU_LOLN**

Fig.4



MT6358 Audio (2/3) Power

- Audio Negative Charge Pump (AUDNCP) related pins: AVDD18_AUD/AVSS18_AUD/AN_V18N/ FLYP/FLYN
  - All traces are wide and short. To minimize ESR and ESL, all traces are on TOP layer without any PCB via. Avoid using PCB VIA between the 5 traces (from ball to cap). (Fig.1 ~ Fig.2)
  - AVSS18_AUD should be connected to main GND with very short trace. (Fig.1 ~ Fig.2)
- AVDD28_AUD and AVSS28_AUD domain, the decoupling cap should also be as close to chip as possible. AVSS28_AUD is connected to main GND with a single VIA. (Fig.3)

Fig.1

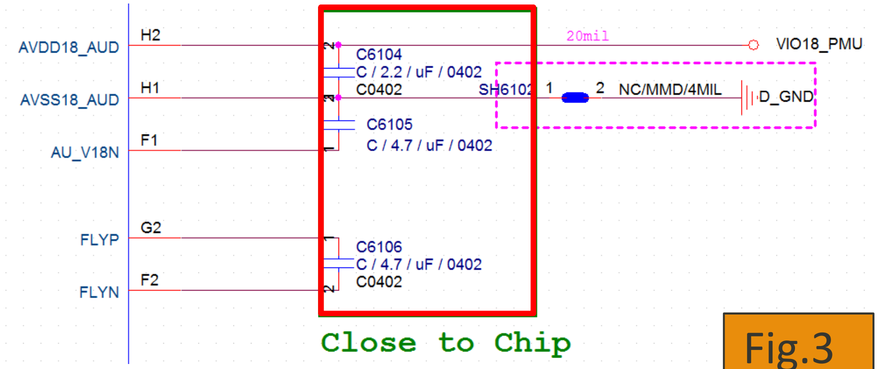


Fig.2

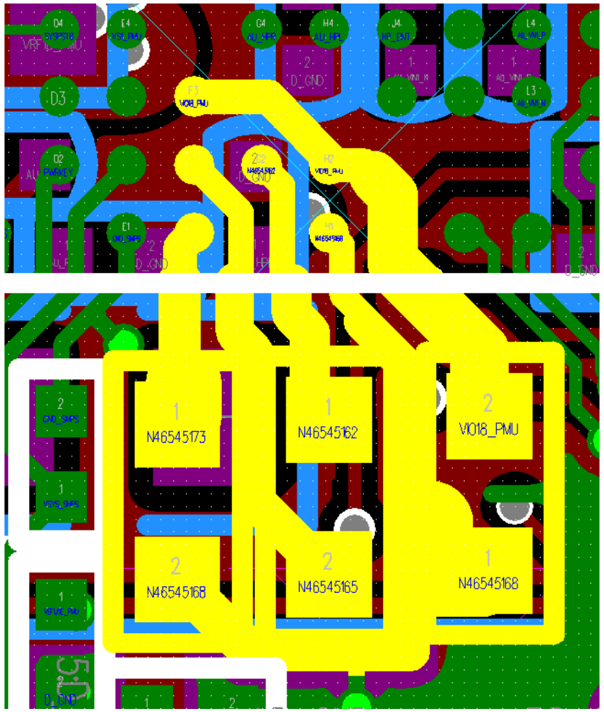
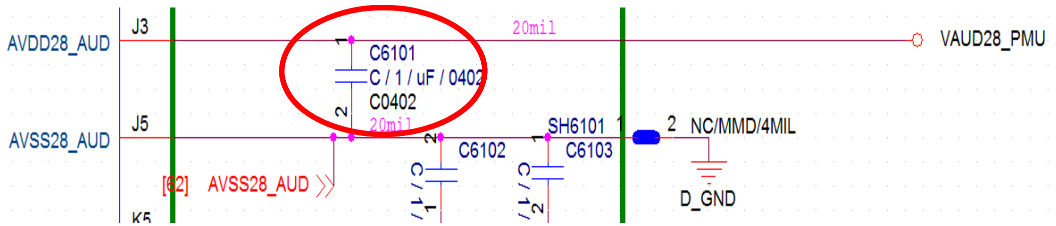


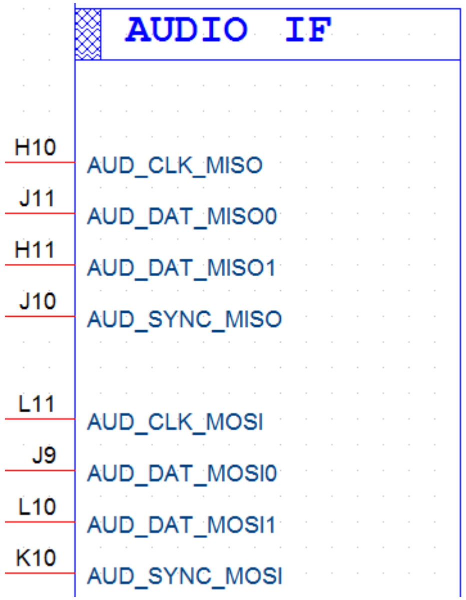
Fig.3



MT6358 Audio (3/3)
Audio/CLK IF Schematic and Layout Notice

- The trace length of AUD_CLK_MOSI/AUD_DAT_MOSI0/AUD_DAT_MOSI1/AUD_SYNC_MOSI should be the same as much as possible.
- The trace length of AUD_CLK_MISO/AUD_DAT_MISO0/AUD_DAT_MISO1/AUD_SYNC_MISO should be the same as much as possible.
- AUD_CLK_MOSI/AUD_CLK_MISO should have GND shielded and the spacing should be >= 3mil.
- Audio IF should be kept away from LX signal (e.g VCORE) and CLK. (Fig. 1)

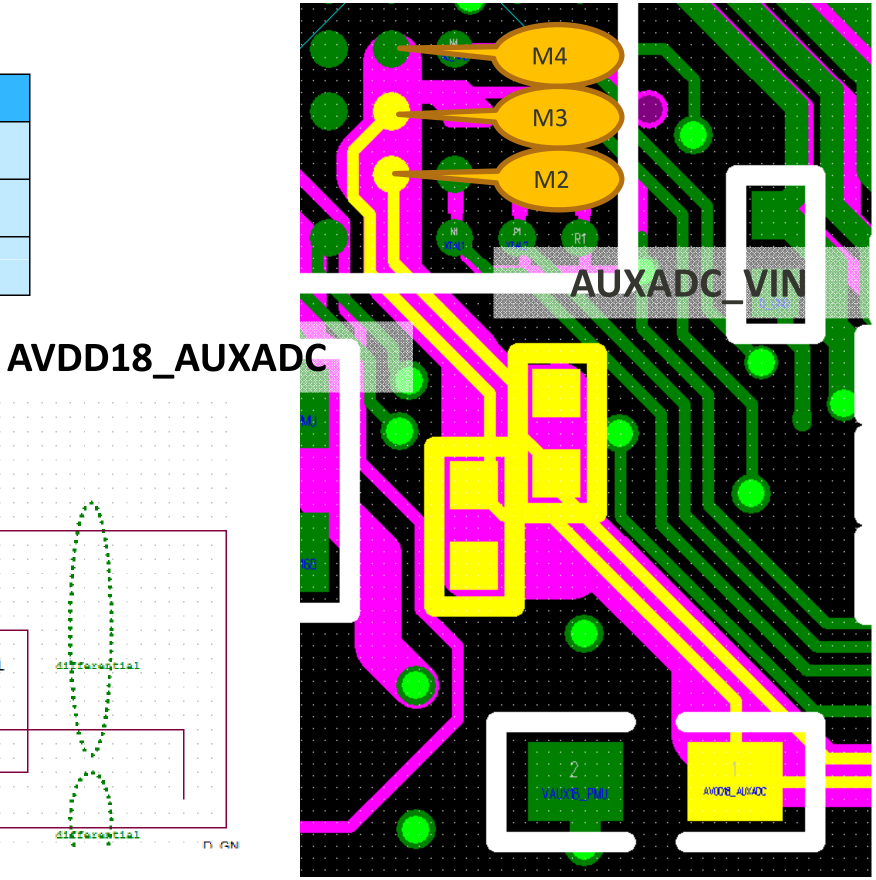
Fig.1

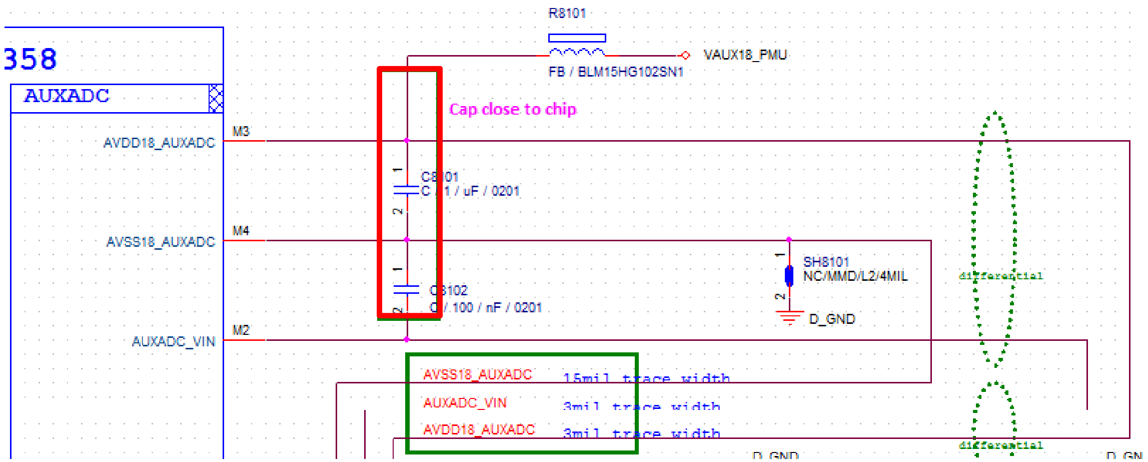


MT6358 AUXADC

- **Recommended AUXADC layout**
  - AVDD18_AUXADC/AUXADC_VIN should be routed as differential pairs with good GND shielding.
  - Route AVSS18_AUXADC with 15 mil trace width under AVDD18_AUXADC/AUXADC_VIN trace to provide return current path.
  - AUXADC capacitor should be placed near AVDD18_AUXADC/AUXADC_VIN pin.

Ball number	IC ball name	PCB net name
M3	AVDD18_AUXADC	AVDD18_AUXADC
M4	AVSS18_AUXADC	AVSS18_AUXADC
M2	AUXADC_VIN	AUXADC_VIN





CONFIDENTIAL B

MT6358 DCXO (1/2)

- XTAL1 and XTAL2 connections to TMS pin1 and pin3 can be swapped. Keep out Buck, NCP, Class-D or other toggling signals 9mm away. (Fig.1)
- Short DCXO gnds to main GND directly by the GND vias. (Fig.2)

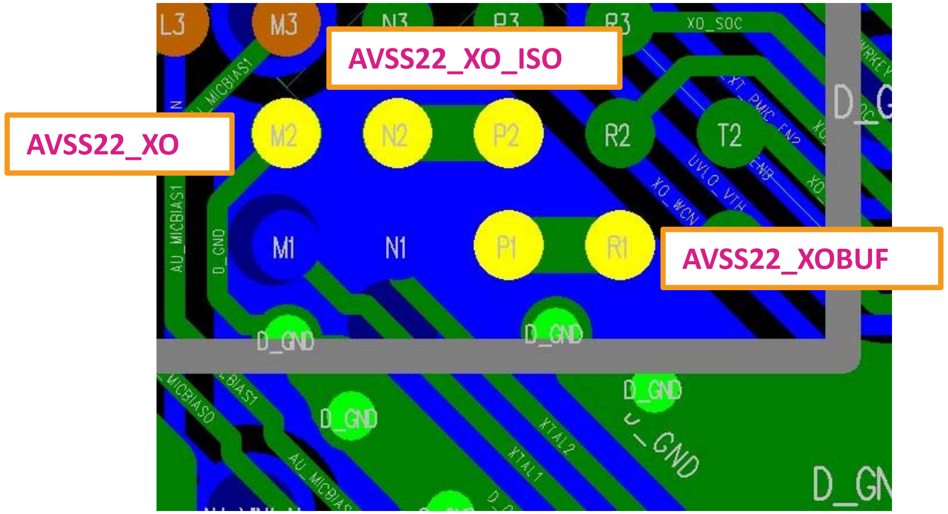
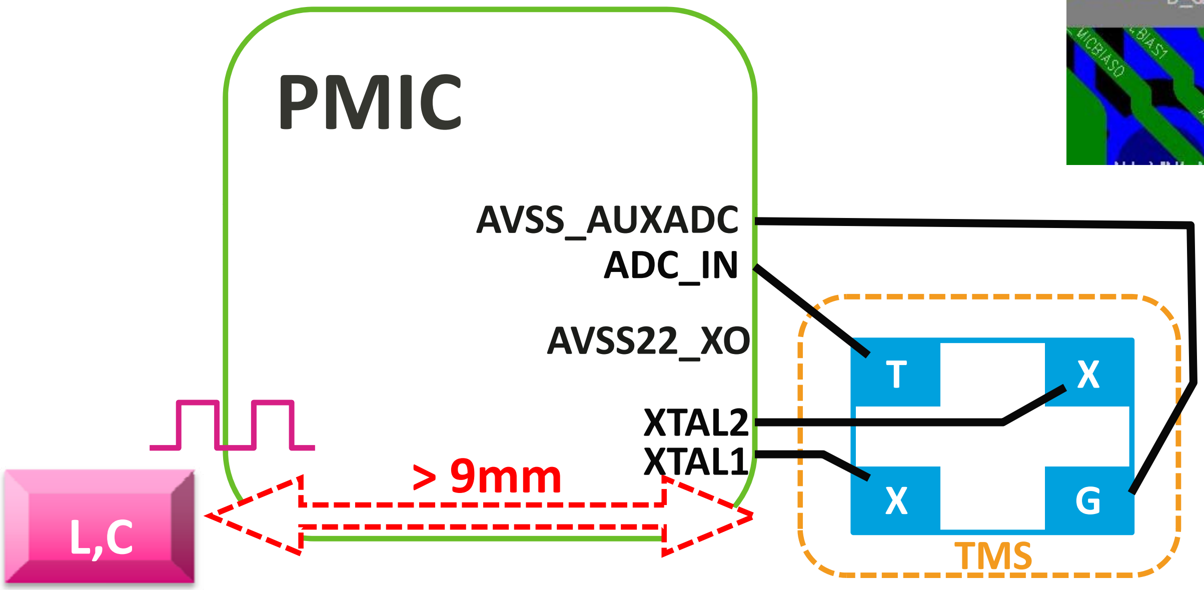


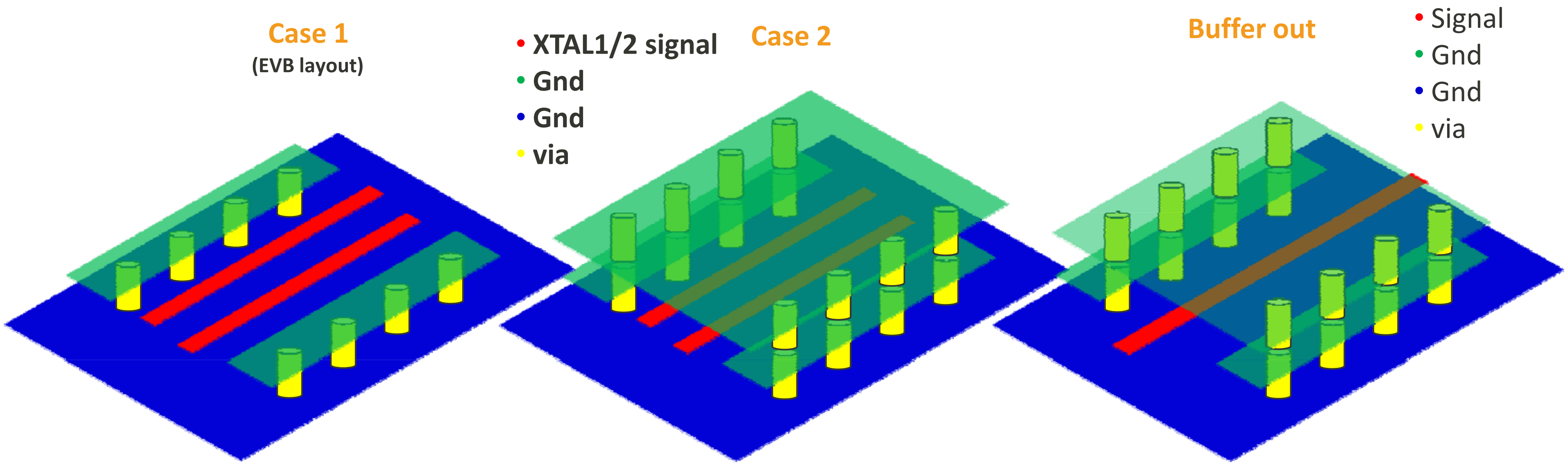
Fig.2

Fig.1



MT6358 DCXO (2/2)

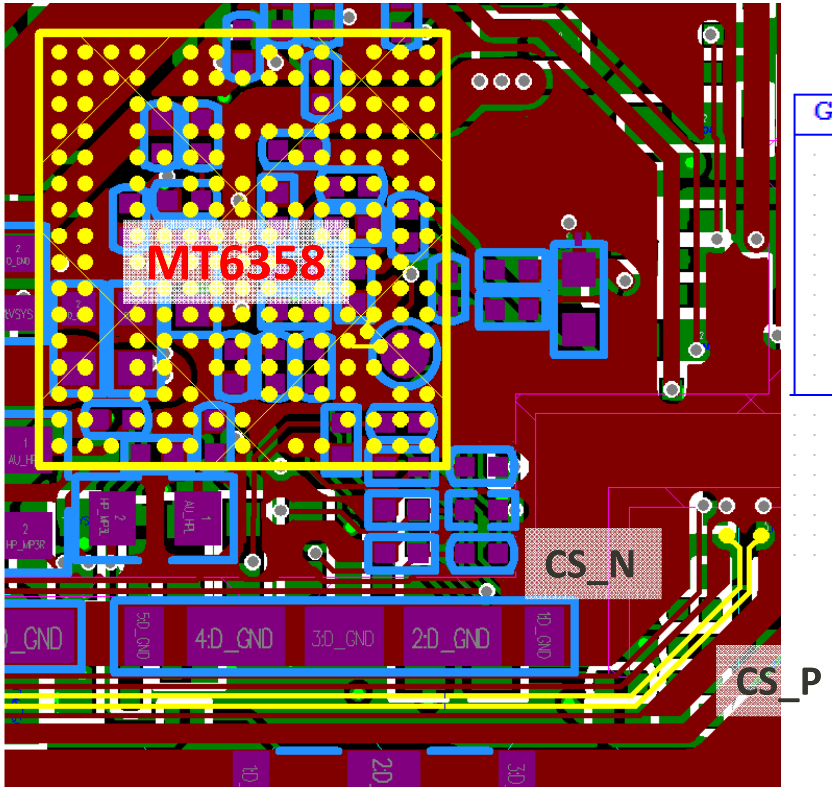
- **XTAL1/2 shielding case 1**
  - Routing XTAL1/2 on 1st layer, and with well-grounding in 1st and 2nd layers.
  - Any other signals crossing or parallel XTAL1/2 are not allowed.
- **XTAL1/2 shielding case 2**
  - Well shielding XTAL1/2 (2nd layer) with GND
  - Any other signals crossing or parallel XTAL1/2 are not allowed.
- Separate ground shielding for each buffer output, XO_SOC, XO_WCN, XO_NFC, XO_CEL, XO_EXT

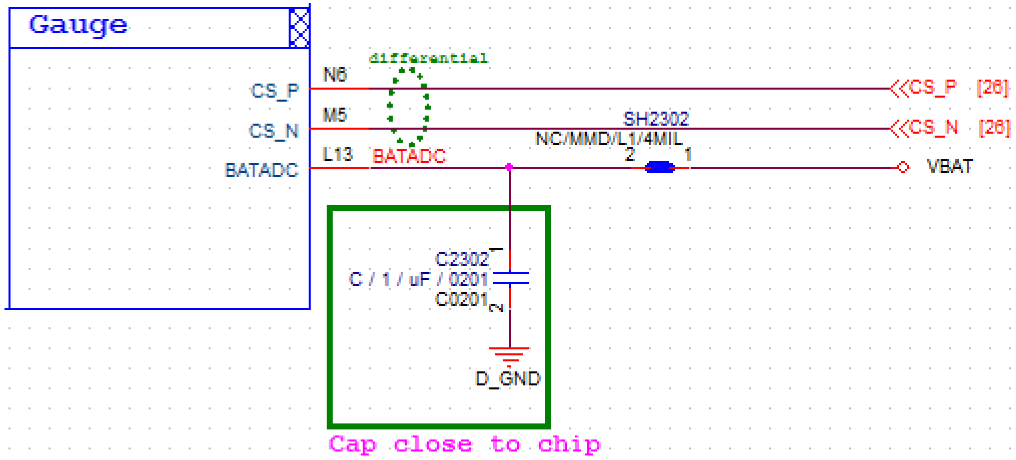


Others for MT6358

Gauge-

- CS_N/CS_P (ball: M5/N6) should be routed as differential pairs and far away from noise signals.



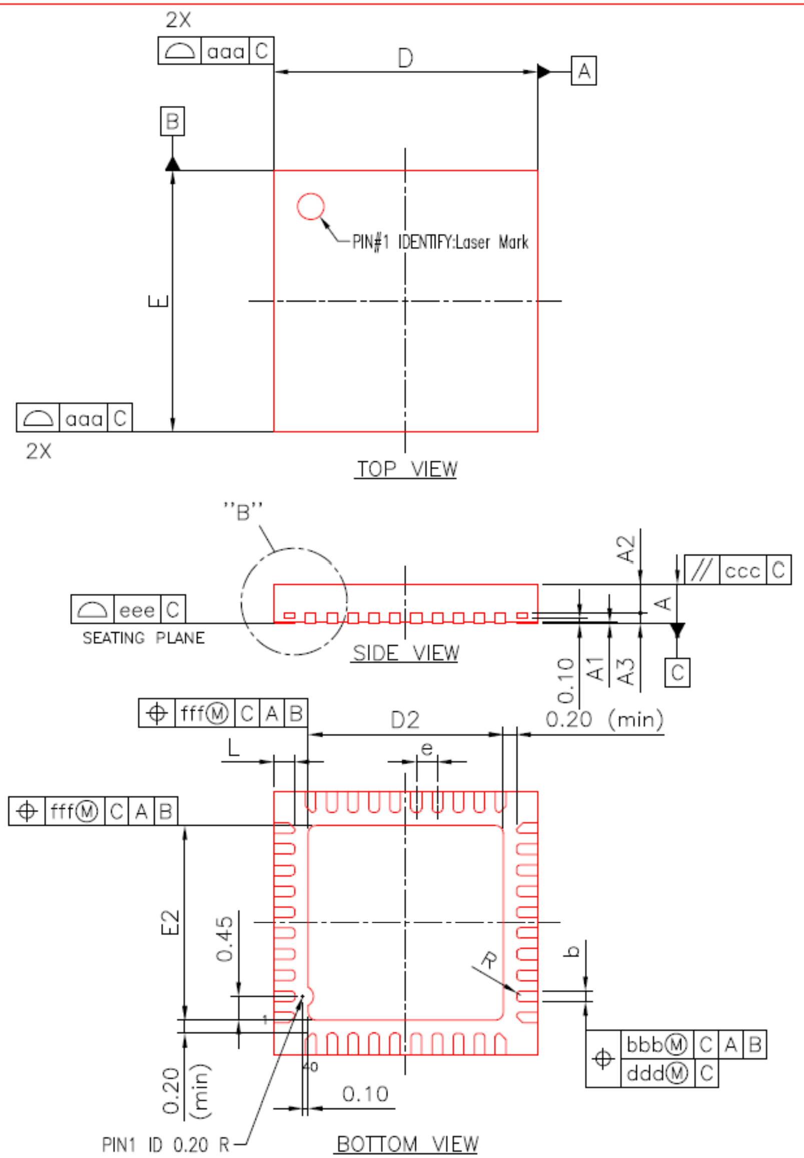


Outlines

- Packaging
  - Package outline of MT6771
  - MT6771 footprint recommendation
  - MT6771 ball out design
- General Guidelines
  - PCB stack-up recommendation
  - Placement notes
- Design Guidelines for High-Speed Digital Signals
  - LPDDR4X/LPDDR3
  - PDN design
- Others
  - MT6177 (RF transceiver)
  - MT6358 (PMU)
  - MT6631 (BT/FM/Wi-Fi/GPS)
  - MT6370 (Battery Charger/USB_PD)
  - eMMC/USB/MIPI/SIM Card/T-Card

MT6631
PCB Layout Guideline

Package Outline of MT6631

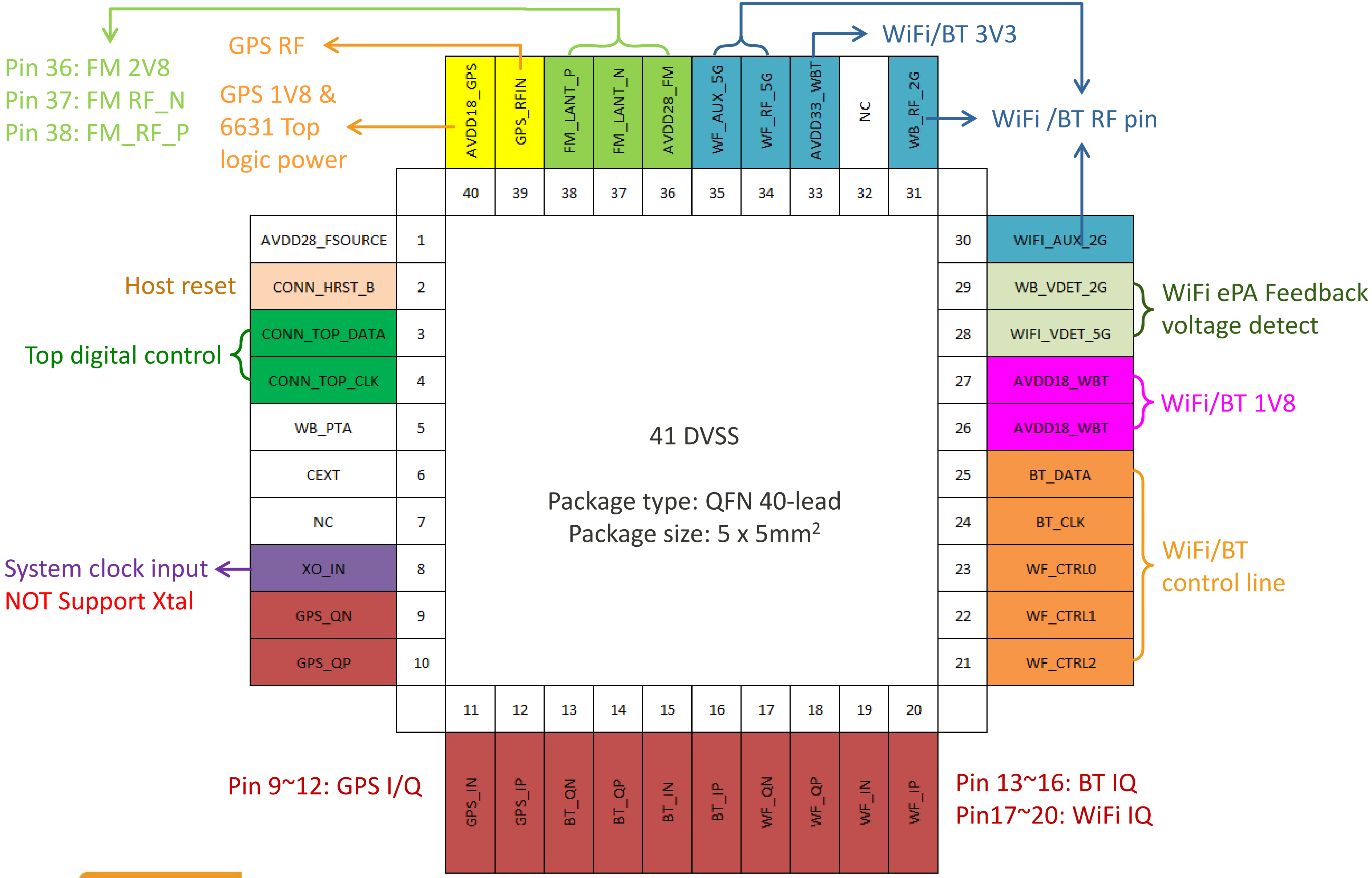


Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.70	0.75	0.80
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.50	0.55	0.60
leadframe thickness		A3	0.20 REF.		
lead width		b	0.15	0.20	0.25
package size	X	D	4.90	5.00	5.10
	Y	E	4.90	5.00	5.10
E–PAD size	X	D2	3.60	3.70	3.80
	Y	E2	3.60	3.70	3.80
lead length		L	0.30	0.40	0.50
lead pitch		e	0.40 bsc		
lead arc		R	0.075	---	---
Package profile of a surface		aaa	0.10		
Lead position		bbb	0.07		
Parallelism		ccc	0.10		
Lead position		ddd	0.05		
Lead profile of a surface		eee	0.08		
Epad position		fff	0.10		

TITLE	PACKAGE OUTLINE 40 L WSQFN 5 X5 X 0.8 mm		MEDIATEK	
	DWG. NO.	REV.	SHEET	UNIT
	MT-SP00329	A	1 OF 2	MM

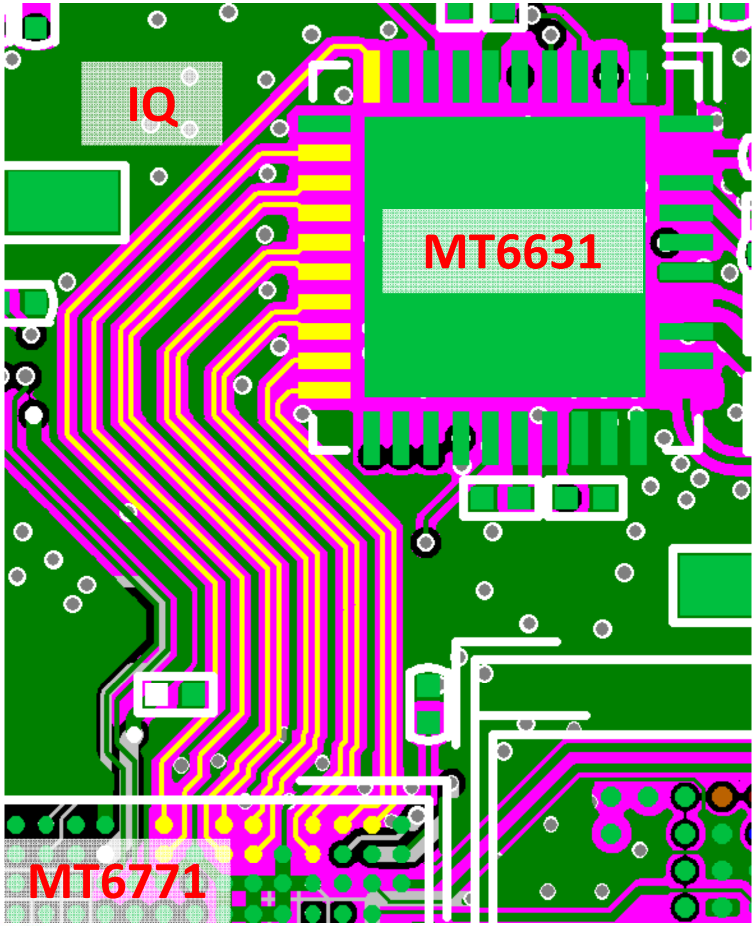
MEDIATEK ADCT Connecting the Future

MT6631 Pin Definition



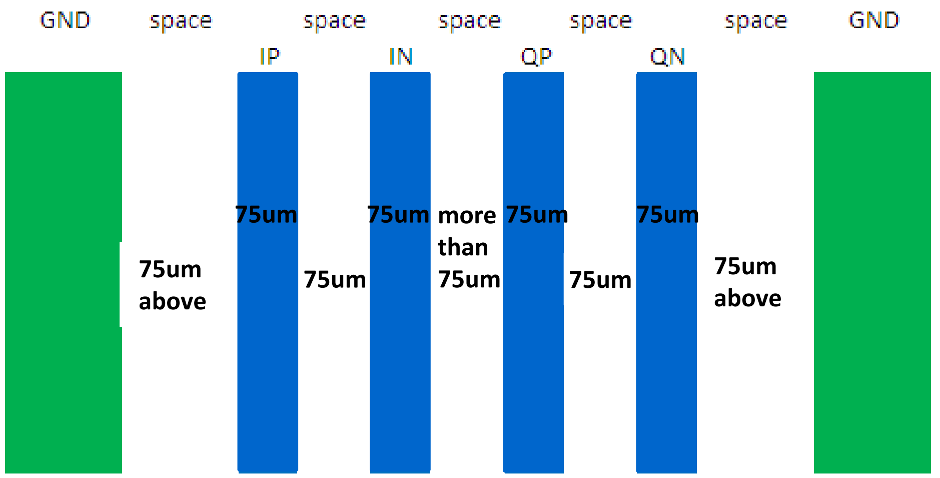
MT6631 v.s. MT6771 Placement

- Keep the distance between MT6631 and MT6771 between 0.7cm~5cm.
  - If < 0.7cm: It may cause connectivity RF de-sense.
  - If > 5cm: IQ signals will be distorted (like EVM fail, Critical).



MT6631 IQ Trace

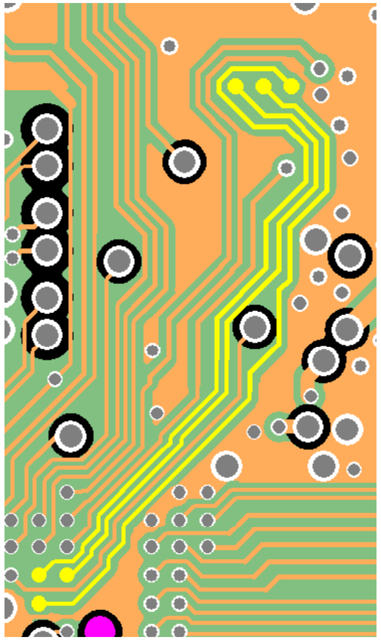
- IQ signals are differential pairs. Every pair should be shielded by GND (adjacent and up/down layers). If the layout area is not enough, shield by groups, for example:
  - WiFi group: WF_IP/IN/QP/QN Pin 17 ~ Pin 20
  - BT group: BT_IP/IN/QP/QN Pin 13 ~ Pin 16
  - GPS group: GPS_IP/IN/QP/QN Pin 9 ~ Pin 12
- IQ trace width/spacing: 75/75um differential pair. PCB trace should be as balanced as possible, and keep differential signals balanced. Smallest differential loop area.
- Spacing 75um~6mil above with GND.



MT6631 Control Trace

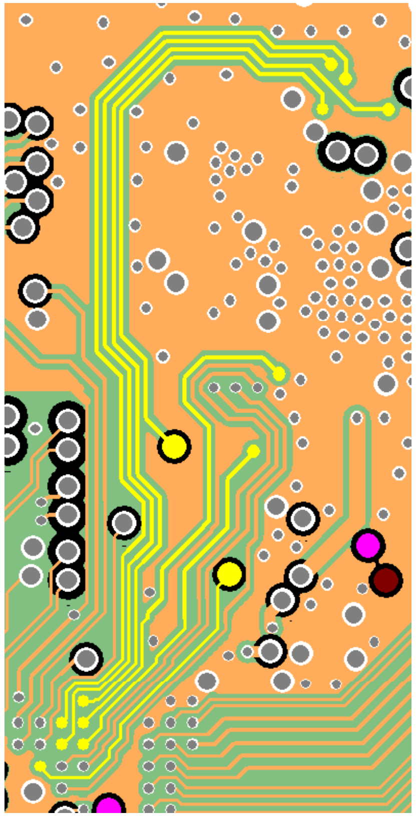
- **High-speed Connectivity WF 3-wire control line**
  - Routed together and shielded by GND for left and right.
  - Do not couple with Power Line and IQ trace, and route in inner layer away from WiFi/GPS RF trace.

Group	Pin no.	PCB net-name
WF_CTRL	23	WF_CTRL0
	22	WF_CTRL1
	21	WF_CTRL2



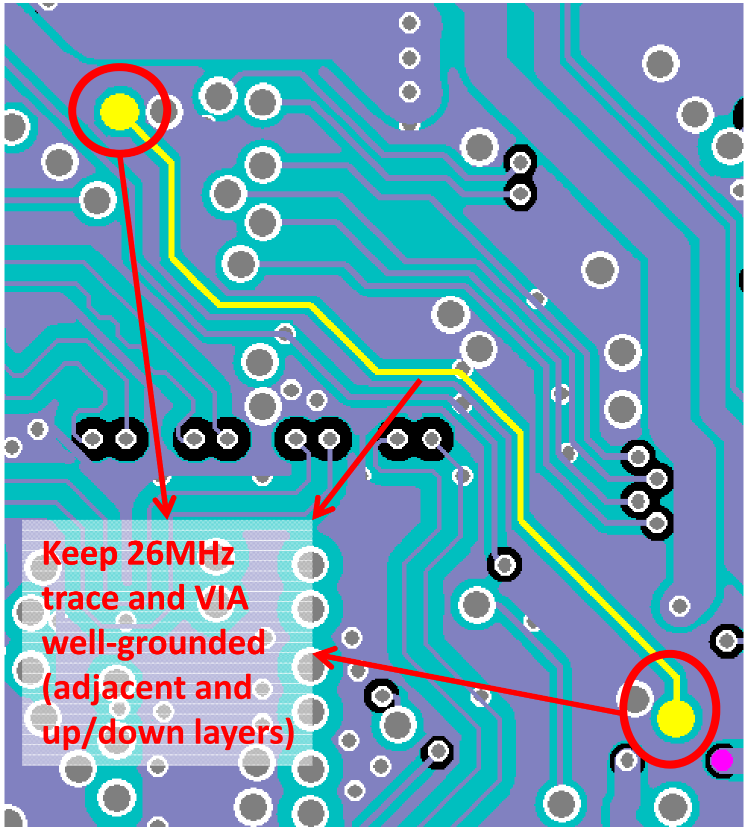
- **Other control signals**
  - Routed in inner layer; do not couple with Power Line and IQ trace.

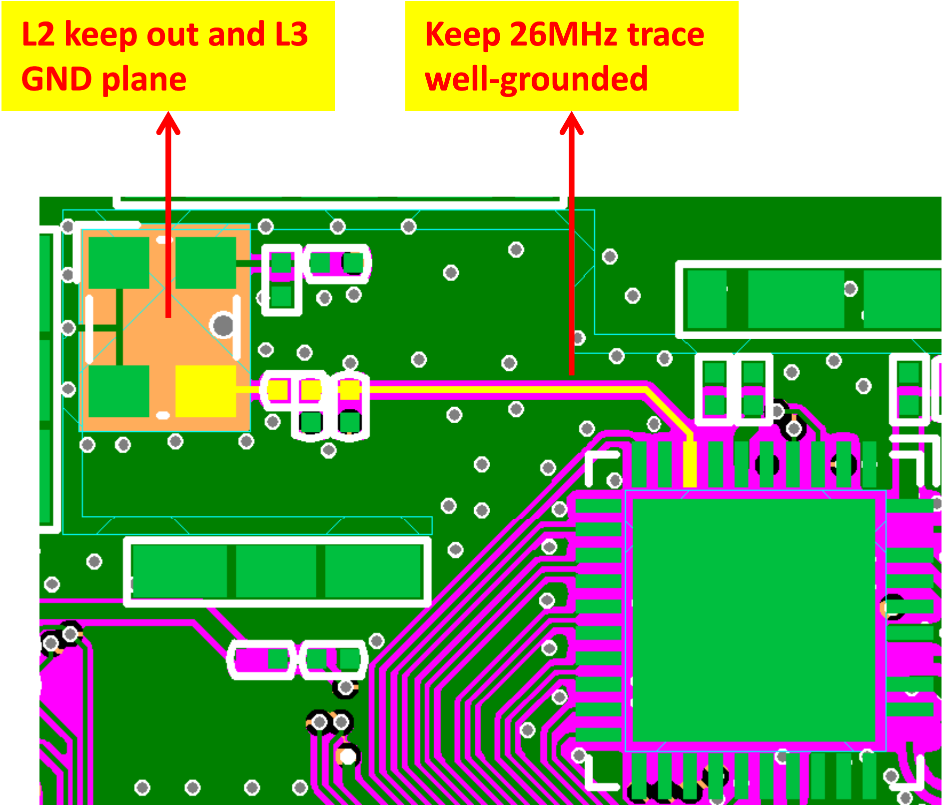
Group	Pin no.	PCB net-name
Other control signals	2	CONN_HRST_B
	3	CONN_TOP_DATA
	4	CONN_TOP_CLK
	5	WB_PTA
	24	BT_CLK
	25	BT_DATA



MT6631 26MHz CLK

- Connectivity 26MHz (pin8: XO_IN) should be shielded by GND and routed far away from noise signals.
- 26MHz trace length should be less than 10cm.
- When adding VIA to change layer, keep VIA in every layer well grounded.
- Keep out the metal on L2 and make GND plane on L3 under all crystal circuits.





MT6631 RF Trace: WiFi/BT/GPS

- WB_RF_2G (pin 31), WB_RF_5G (pin 34) and GPS_RFIN (pin 39) are RF antenna pin for WiFi/BT/GPS. Keep **50Ω impedance** with good shielding by GND. (Fig.1)
- Route on L1 and avoid layer transition for RF trace route (affect impedance control and PCB trace loss). (Fig.1)
- MT6631 must be placed close to Wi-Fi antenna (make RF trace short, Wi-Fi 5GHz PCB trace loss is huge). (Fig.1~2)
- GPS external LNA components must be close to antenna and route on Layer 1. (Fig.1~2)

Fig.1

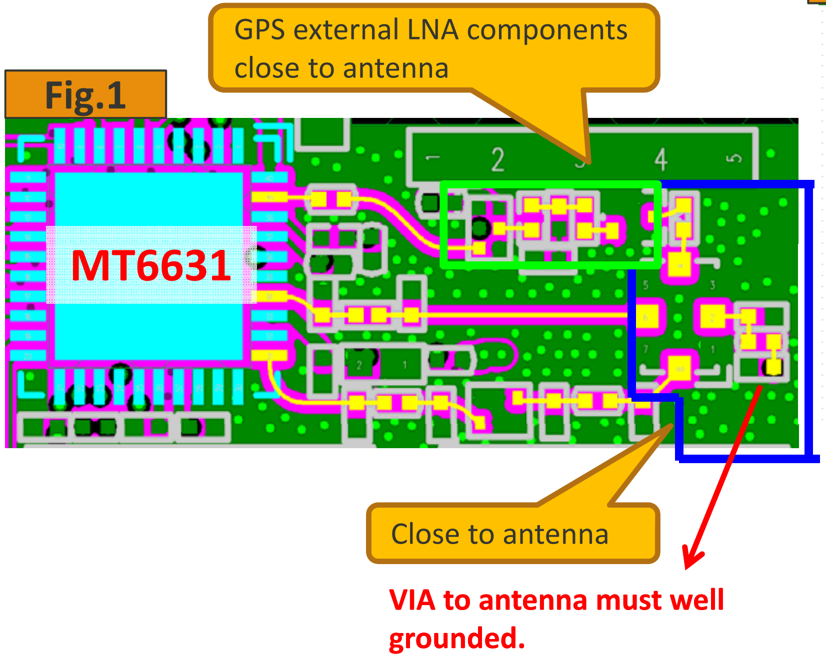
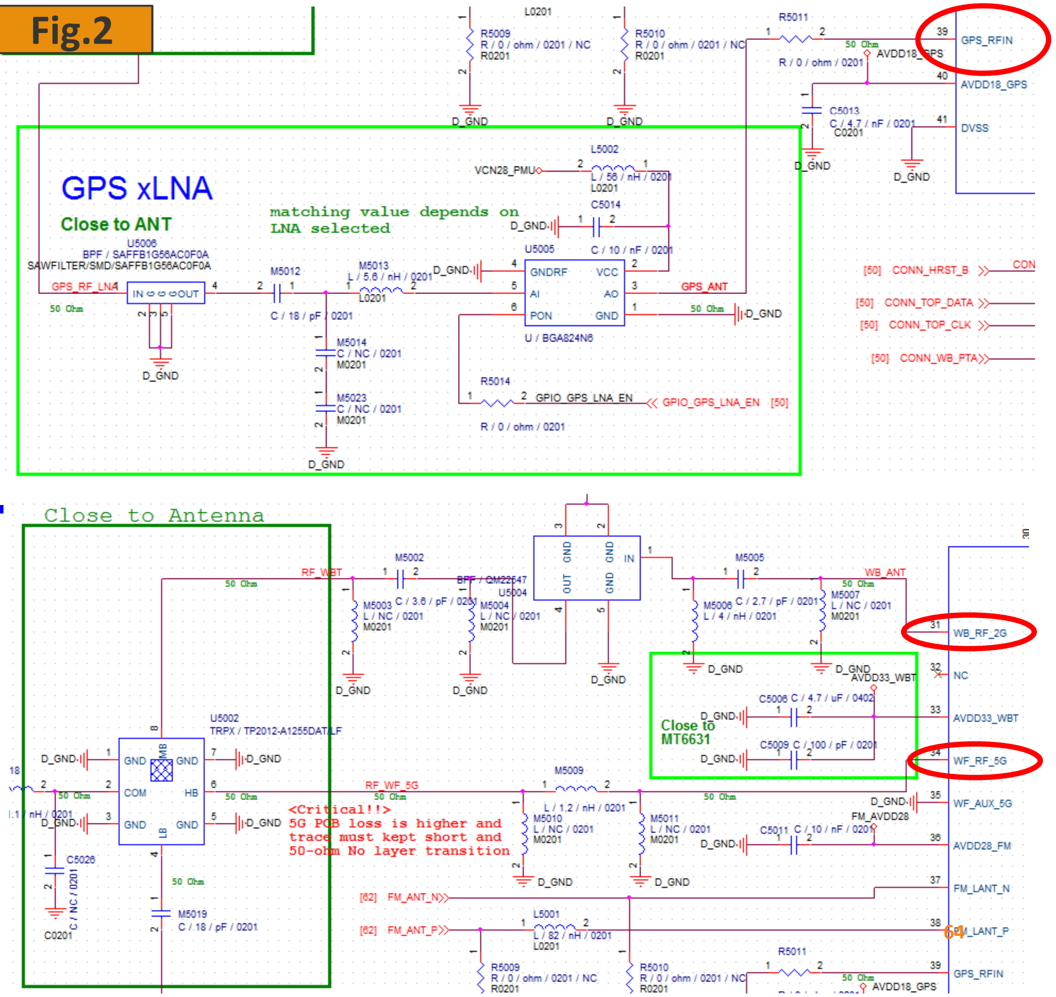
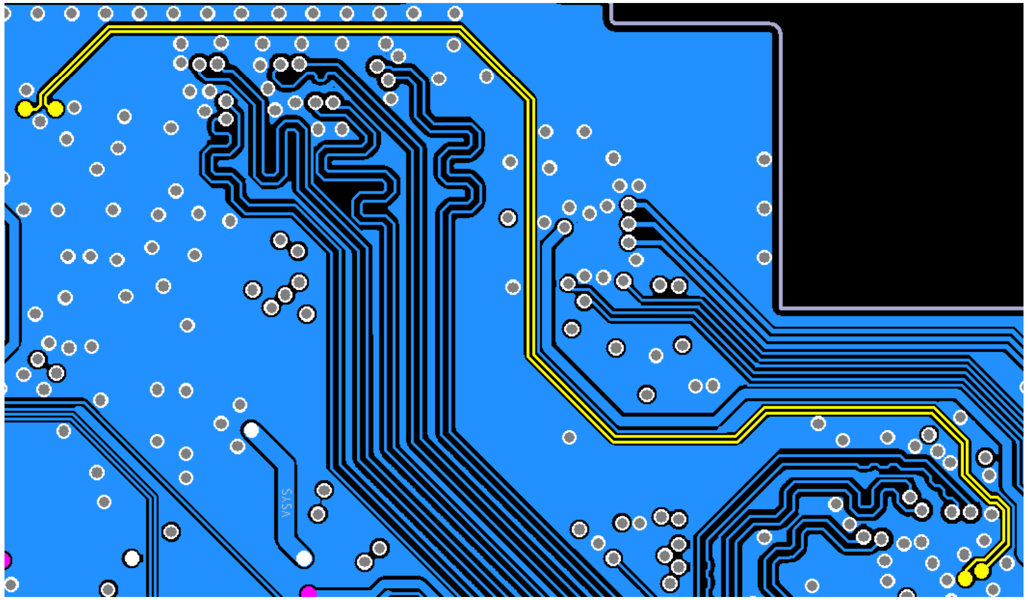


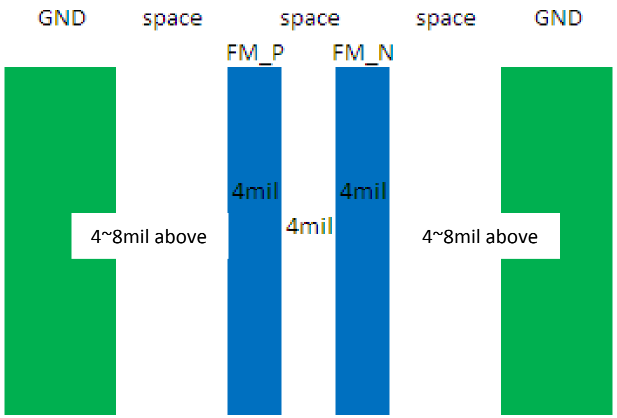
Fig.2

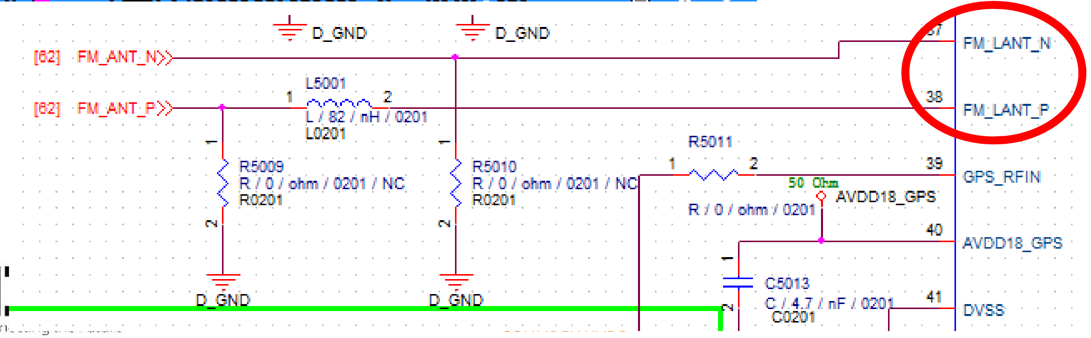


MT6631 RF Trace: FM

- FM_LANT_N (pin 37) and FM_LANT_P (pin 38) are FM signals and required for differential pairs to get better noise immunity.
- FM signals must be shielded by GND (left/right /upper/lower) with stitching GND via.
- If RF trace cannot be well protected, it will produce noise to FM easily.
- ESD interference can be avoided if FM trace is in the inner layer and has good GND shielding.







MT6631 Power Trace (1/2)

- AVDD33_WBT: Place decupling capacitors close to power pin 33. (Fig.1, 3)
- AVDD28_FM: Place decupling capacitors close to power pin 36. (Fig.1~2)
- Keep away from other noisy power traces and high speed digital traces.

Fig.1

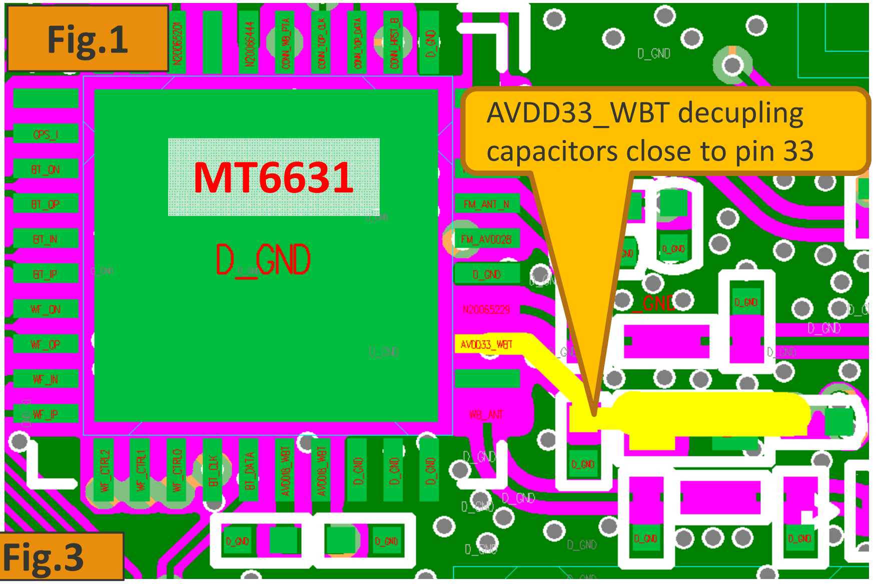


Fig.2

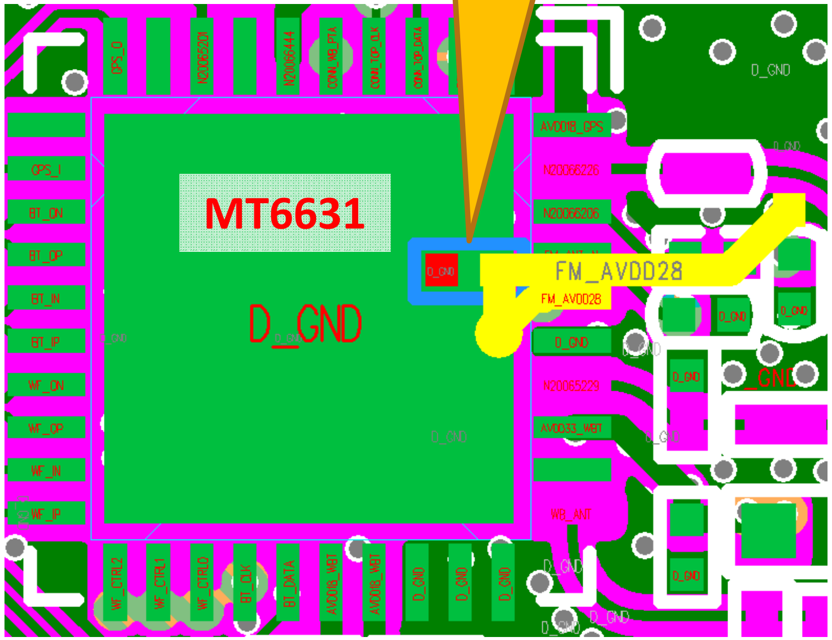
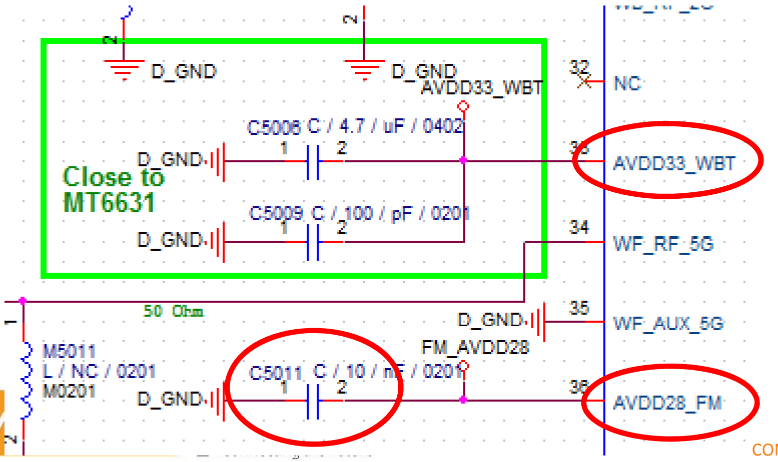


Fig.3



CONFIDENTIAL B

MT6631 Power Trace (2/2)

- AVDD18_WBT: Place decupling capacitors close to power pin 26,27. (Fig.1~2)
- AVDD18_GPS: Place decupling capacitors close to power pin 40. (Fig.1 、3)
- Power traces VCN18_PMU should be used star routing topology to connect AVDD18_WBT (pin 26,27) and AVDD18_GPS (pin 40). (Fig.1)
- Keep away from other noisy power trace and high speed digital trace.

Fig.1

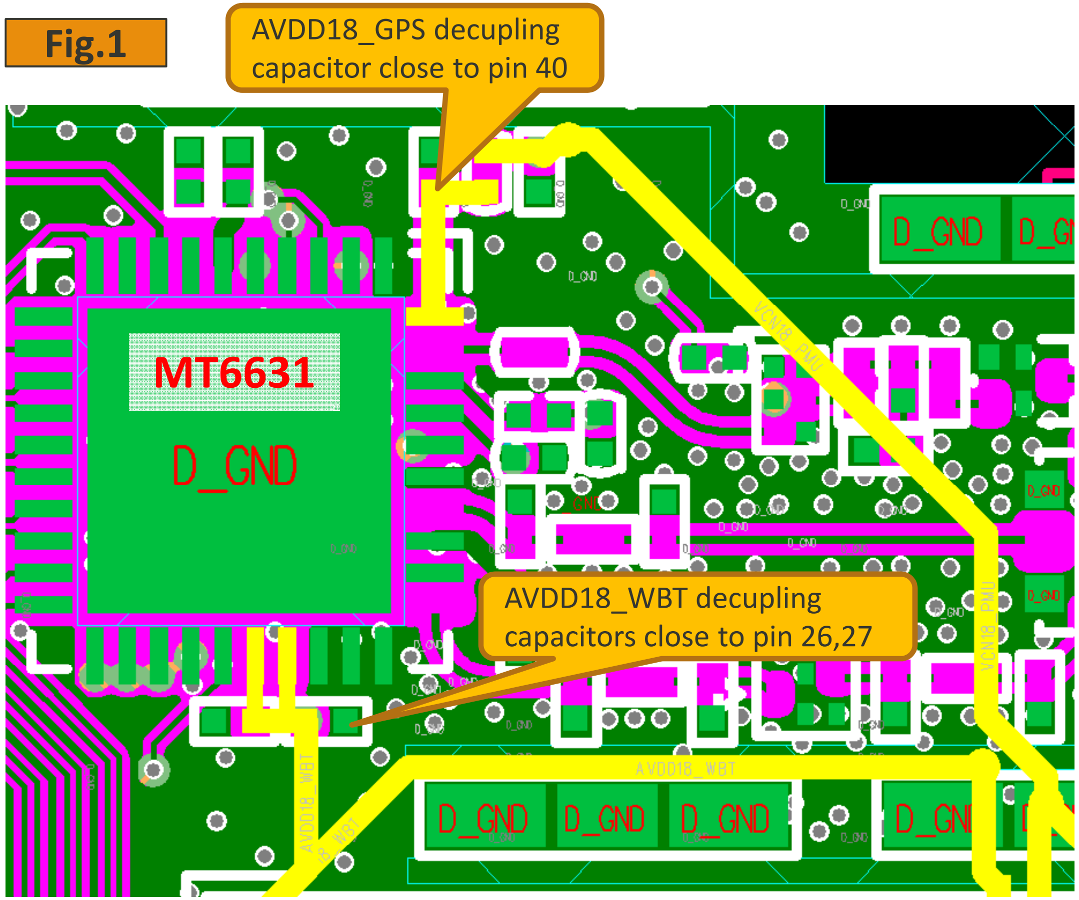


Fig.2

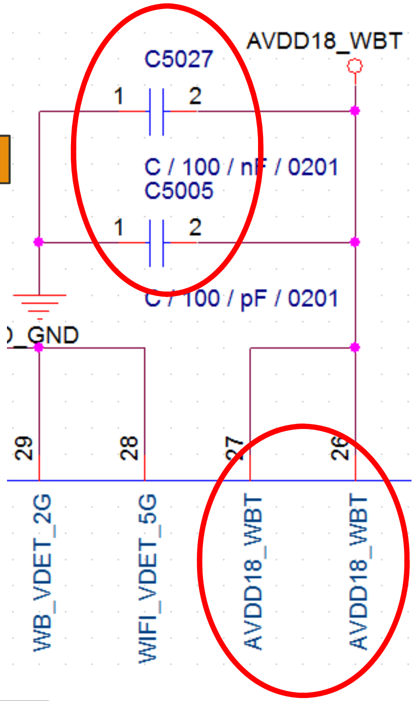
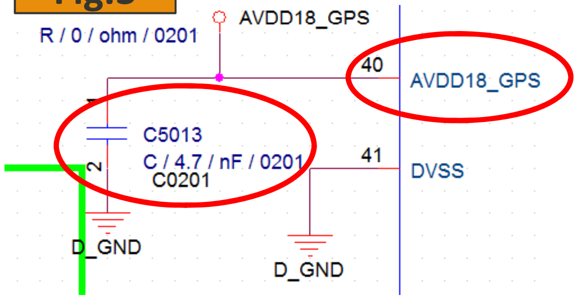


Fig.3



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  - eMMC/USB/MIPI/SIM Card/T-Card

MT6370
PCB Layout Guideline

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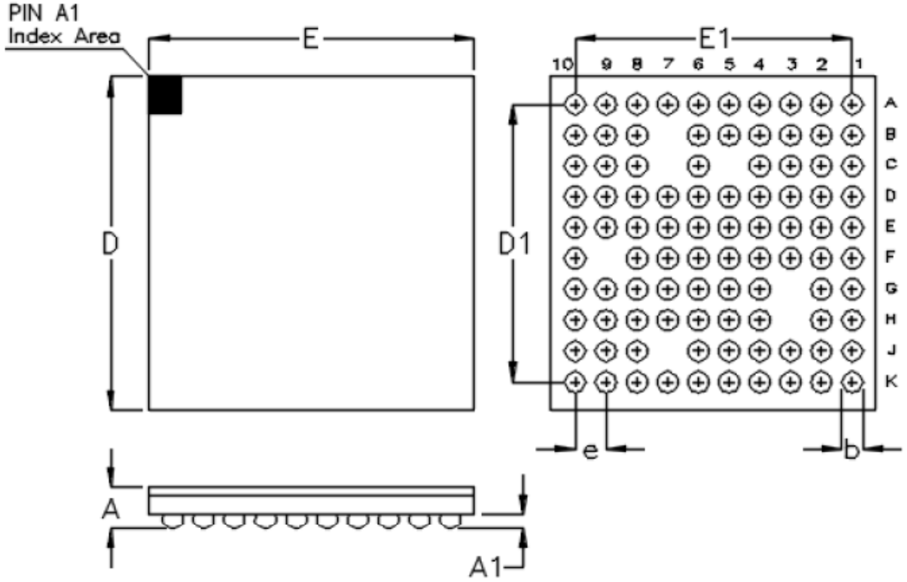
CONFIDENTIAL B

Package Outline of MT6370



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	4.280	4.360	0.169	0.172
D1	3.600		0.142	
E	4.180	4.260	0.165	0.168
E1	3.600		0.142	
e	0.400		0.016	

93B WL-CSP 4.22x4.32 Package (BSC)

MT6370 Pin Definition

(TOP VIEW)

A1 CHG_VIN	A2 CHG_VIN	A3 CHG_VIN	A4 D-	A5 D+	A6 FL_LEDCS2	A7 FL_LEDCS1	A8 PD_VBUS	A9 PD_CC2	A10 BL_VLX
B1 CHG_VMID	B2 CHG_VMID	B3 CHG_VMID	B4 FL_VMID	B5 FL_VMID	B6 FL_VMID		B8 PD_IRQB	B9 PD_VCONN5V	B10 BL_PGND
C1 CHG_VLX	C2 CHG_VLX	C3 CHG_VLX	C4 NC		C6 FL_VINTORCH		C8 CHG_ILIM	C9 PD_CC1	C10 BL_VDDA
D1 CHG_PGND	D2 CHG_PGND	D3 CHG_PGND	D4 CHG_BOOT	D5 VBATS	D6 FL_STROBE	D7 FL_TORCH	D8 CHG_OTG	D9 BL_VOUT	D10 BL_LED1
E1 VSYS	E2 VBUS	E3 CHG_VDDP	E4 OVP_CTRL	E5 AGND	E6 AGND	E7 AGND	E8 CHG_QONB	E9 CHG_ENB	E10 BL_LED2
F1 VSYS	F2 VSYS	F3 CHG_VBATOVPB	F4 NC	F5 AGND	F6 AGND	F7 AGND	F8 CHG_DSEL		F10 BL_LED3
G1 VBAT	G2 VBAT		G4 CHG_STAT	G5 AGND	G6 AGND	G7 AGND	G8 FL_TXMASK	G9 AGND	G10 BL_LED4
H1 VBAT	H2 VBAT		H4 RGB_ISINK4	H5 RGB_ISINK1	H6 DB_ENN	H7 DB_ENP	H8 MRSTB	H9 BL_PWM	H10 BL_EN
J1 LDO_VOUT	J2 LDO_VIN	J3 TS	J4 RGB_ISINK3	J5 RGB_ISINK2	J6 IRQB		J8 SCL	J9 SDA	J10 VDDA
K1 DB_NEGVOUT	K2 DB_NEGCF2	K3 DB_NEGPGND	K4 DB_NEGCF1	K5 DB_POSVOUT	K6 DB_BSTVOUT	K7 DB_POSVLX	K8 DB_POSPGND	K9 VDDM	K10 DB_VDDA

WL-CSP-93B 4.22x4.32 (BSC)

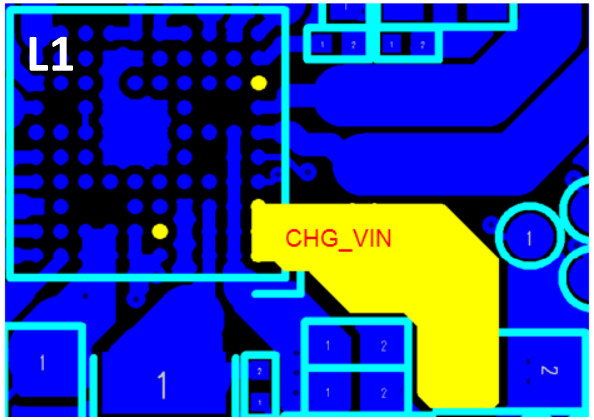
MT6370 Schematic/Layout Notice

- High current path must enlarge trace width as 25mil/1A.
  - CHG_VIN, CHG_VLX, VSYS and VBAT→4A
  - CHG_VMID, FL_VMID→2.5A
  - FLED1/2→1.5A
- Bypass CAP/Resistor near to related ball.
  - VDDM, VDDA, BL_VDDA, DB_VDDA, CHG_BOOT to CHG_VLX, and CHG_ILIM.
- Inductor close to LX pins and not couple to another sensitive trace.(ex: SDA/SCL)
- VDDM and VDDA, BL_VDDA and DB_VDDA cap's GND should be directly connected to GND plane.

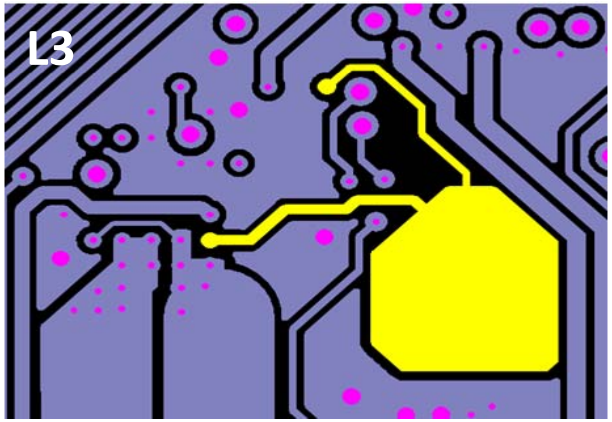
CONFIDENTIAL B

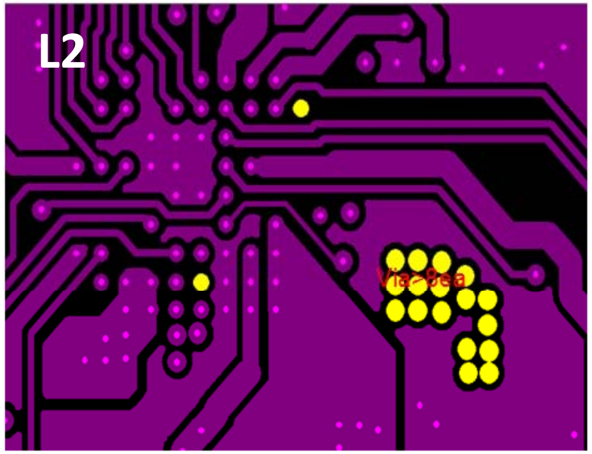
MT6370 - Charger CHG_VIN Trace

- High current path CHG_VIN, CHG_VLX, VSYS and VBAT→4A

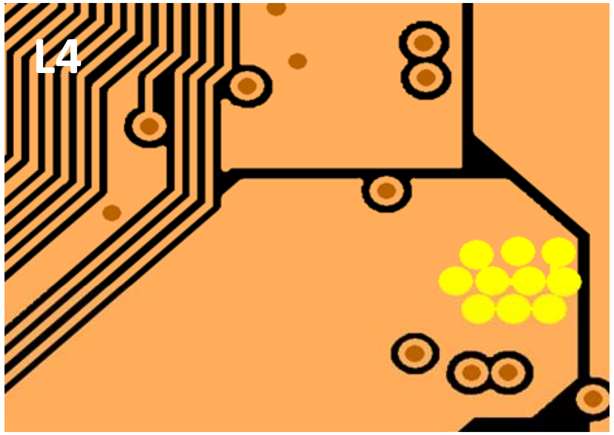


L1:CHG_VIN trace must be > 2.5mm



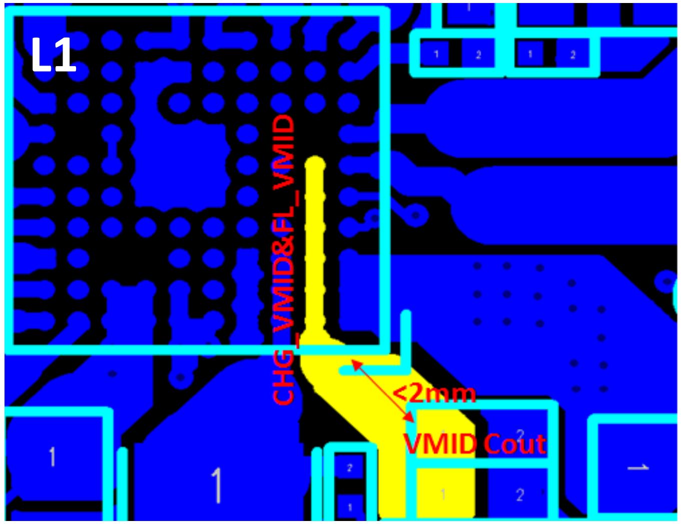


L2: Via numbers should be >8ea for current path.

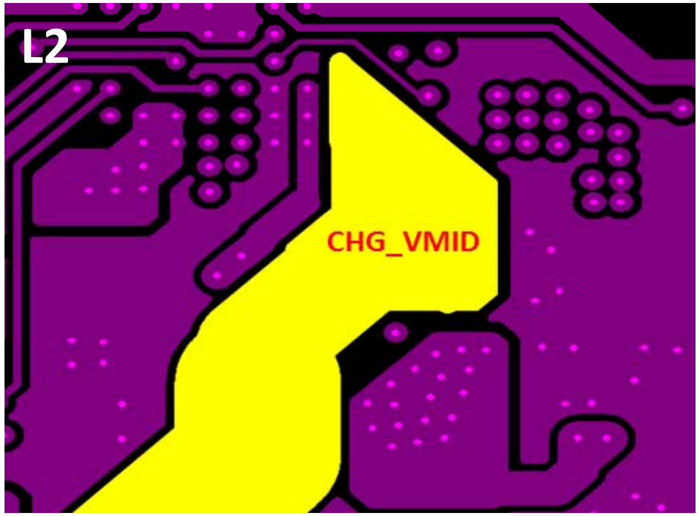


L4: CHG_VIN trace must be > 2.5mm

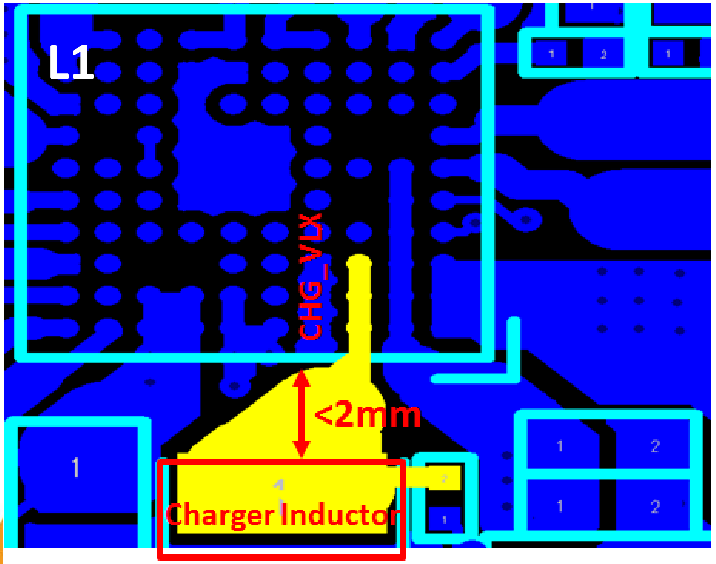
MT6370 - Charger CHG_VMID & CHG_VLX



CHG_VMID Output Cap
place as close to IC(<2mm)

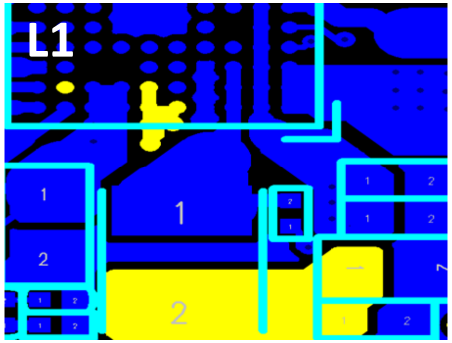


CHG_VMID(=FL_VMID) trace must be > 1.5mm
for parallel charger application

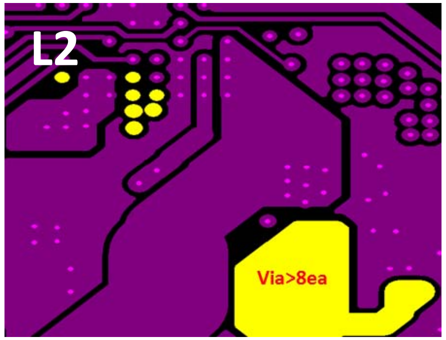


CHG_VLX Inductor
place as close as possible to IC(<2mm)

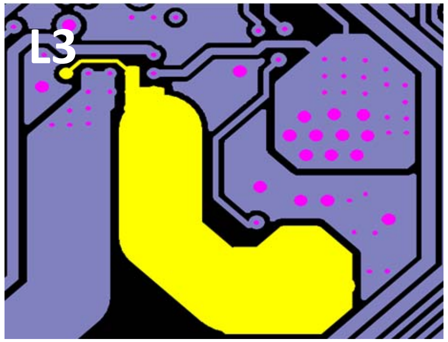
MT6370 – VSYS & VBAT



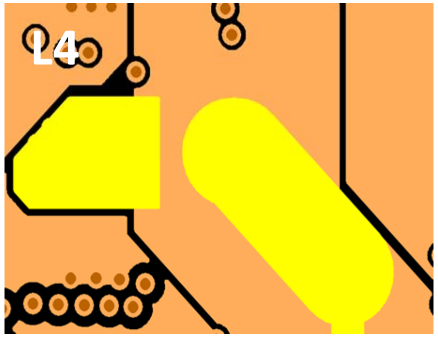
VSYS trace
must be > 2.5mm



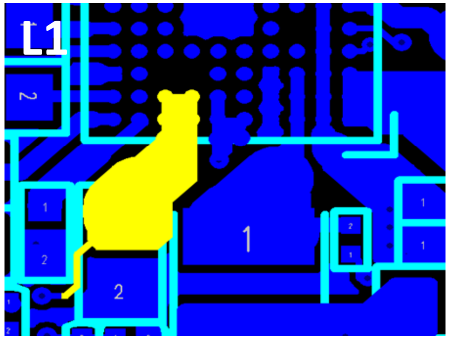
VSYS-Via should be
>8ea for current path.



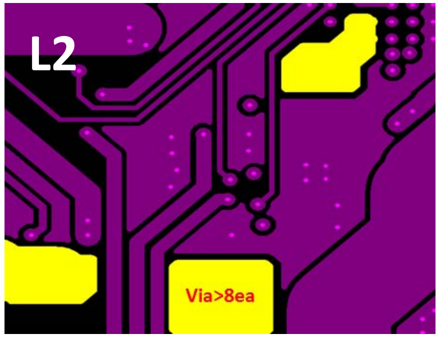
VSYS trace
must be > 2.5mm



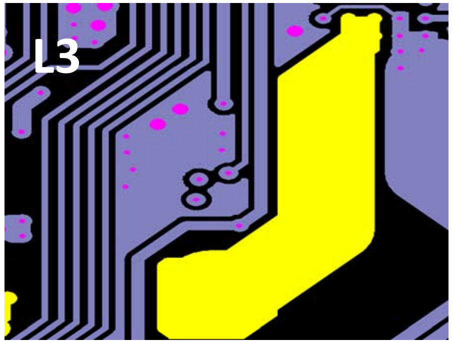
VSYS trace
must be > 2.5mm



VBAT trace
must be > 2.5mm

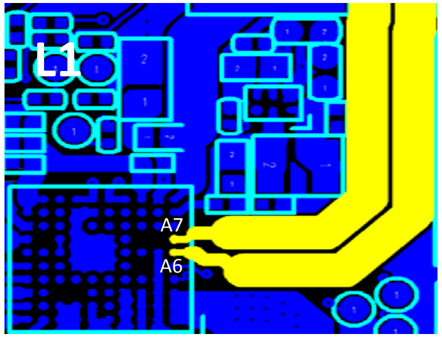


VBAT-Via should be
>8ea for current path.

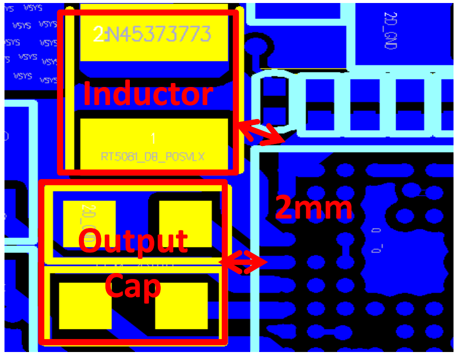


VBAT trace
must be > 2.5mm

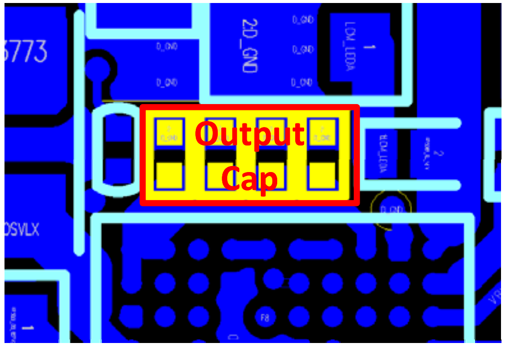
MT6370 – FLED/ Display / VDDM



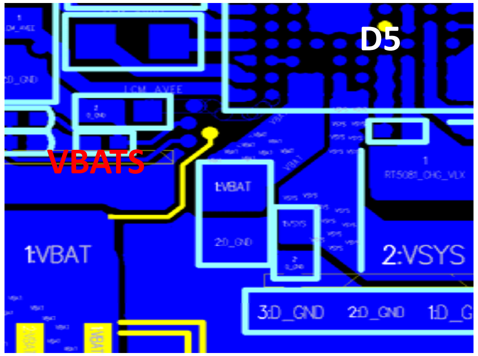
FLED1/FLED2(Pin:A6,A7)
trace must be > 750um



Display Bias (Pin:K7)
Inductor and Output Cap Close to IC <2mm



VDDM/ VDA
Output Cap Close to IC <2mm
These output caps' GND should be isolated from the nearby GND trace and plane then connected to main GND directly.



VBATS (Pin:D5) sense trace
must connect to VBAT - battery pack side.

Outlines

- **Packaging**
  - Package outline of MT6771
  - MT6771 footprint recommendation
  - MT6771 ball out design
- **General Guidelines**
  - PCB stack-up recommendation
  - Placement notes
- **Design Guidelines for High-Speed Digital Signals**
  - LPDDR4X/LPDDR3
  - PDN design
- **Others**
  - MT6177 (RF transceiver)
  - MT6358 (PMU)
  - MT6631 (BT/FM/Wi-Fi/GPS)
  - MT6370 (Battery Charger/USB_PD)
  - eMMC/USB/MIPI/SIM Card/T-Card

eMMC/UFS/USB/MIPI/ SIM Card/T-Card

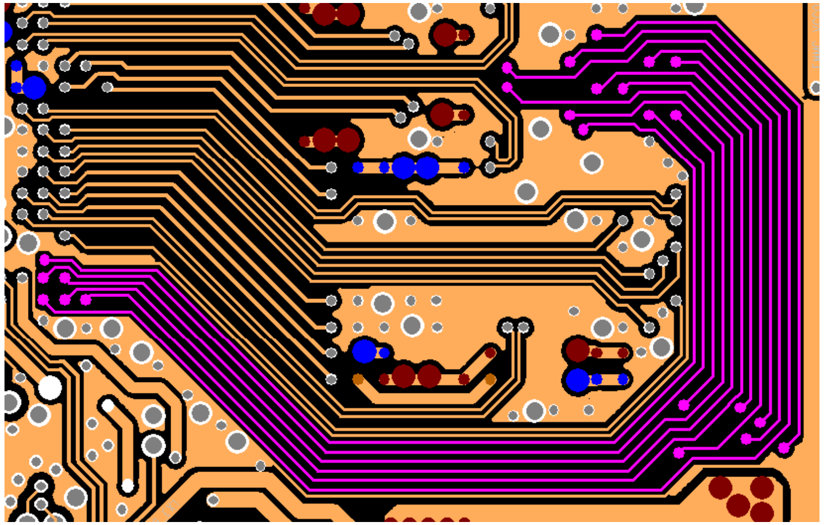
eMMC 5.x

BreakOut Region Topology:

Main routing on L1/L3, L2/L4 solid reference gnd:

Breakout length ≦ 3810 um (as short as possible)

- A. Keep L2 as solid reference gnd as possible.
- B. Place the gnd stitching via between BGA ball and L2 gnd on both AP/eMMC.
- C. Trace Width (w) = Minimum Trace Width
- D. Trace Spacing ≧ W um



Main Route Region Topology:

Main routing on L1/L3, L2/L4 solid reference gnd:

Trace length <=50800 um

- A. Trace Width (w) = W um
- B. Trace Spacing:
  1. DATA to DATA ≧ 2Wum
  2. CLK to DATA/CMD/DSL/RST ≧ 2W um
  3. DSL to DATA/CMD/CLK/RST ≧ 2W um
  4. CMD to DATA/CLK/DSL/RST ≧ 2W um
  5. RST to DATA/CLK/DSL/CMD ≧ 2W um

Length matching:

- A. |Clock – Data/CMD| ≦ 7620 um
- B. |DSL – Data/CMD| ≦ 7620 um

PI : PCB Decap location

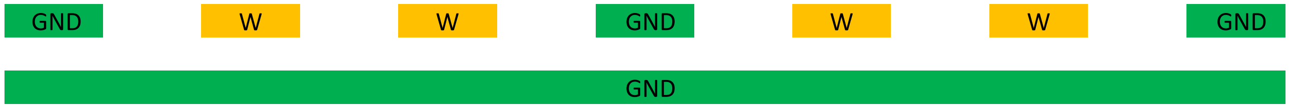
- A. Distance to SOC ≦ 3810 um
- B. Trace width (W) ≧ 200 um
- C. Cap Value ≧ 0.1 uF

MEDIATEK ADCT Connecting the Future

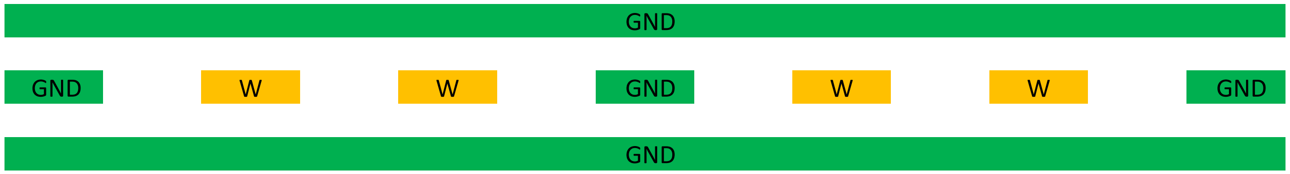
UFS

- Differential pairs are well-shielded by GND (adjacent and up/down layers).

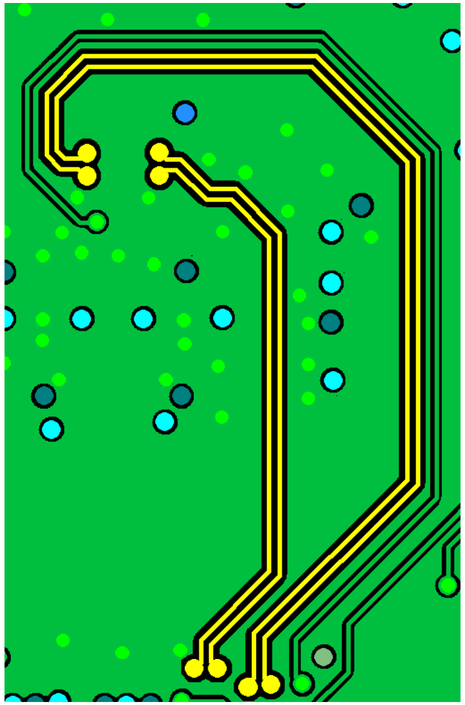
	Differential impedance	P/N skew	Total length	Number of vias allowed
UFS_TX0P/N, UFS_RX0P/N	100ohm	< 5mil	< 6 inch	2



Outer layer



Inner layer

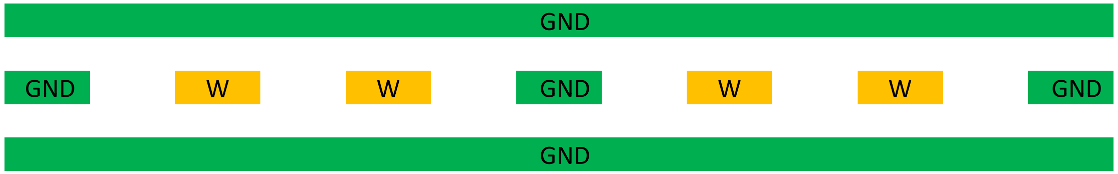


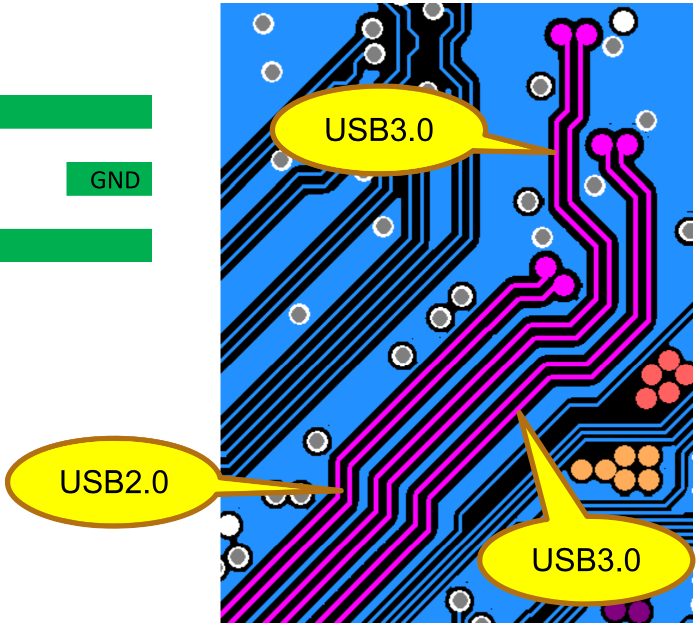
USB 2.0/USB 3.0

- Differential pairs are well-shielded by GND and GND vias (adjacent and up/down layers).
- Routing differential pair straight and symmetrically on the same layer.
- USB2.0: Maximum of 2 via-hole/layer change. USB3.0: no via preferred

	Differential impedance	P/N skew*	Total length
USB_DP/DM	90ohm	< 1.5mm	< 8inch
SSUSB_TXP/TXN, SSUSB_RXP/RXN	90ohm	< 125um	< 5inch

* Related to common mode noise





- If there is switch/FPC for
USB 2.0, keep IL < 2dB @ 240MHz
USB 3.0, keep IL < 3dB @ 2.5GHz

MIPI - DPHY

- MIPI signals’ differential impedance: 100Ω
- Total length < 6 inch (PCB + FPC + Module)
  - Lane-to-clock matching ≤ 2.5mm
  - P/N skew ≤ 625um
- Well shielded by GND (adjacent and up/down layers) is recommended; otherwise keep the spacing ≧ 3x min (h1, h2) rule. (Fig. 1&2)
- Ground isolation (adjacent and up/down layers) from other signals

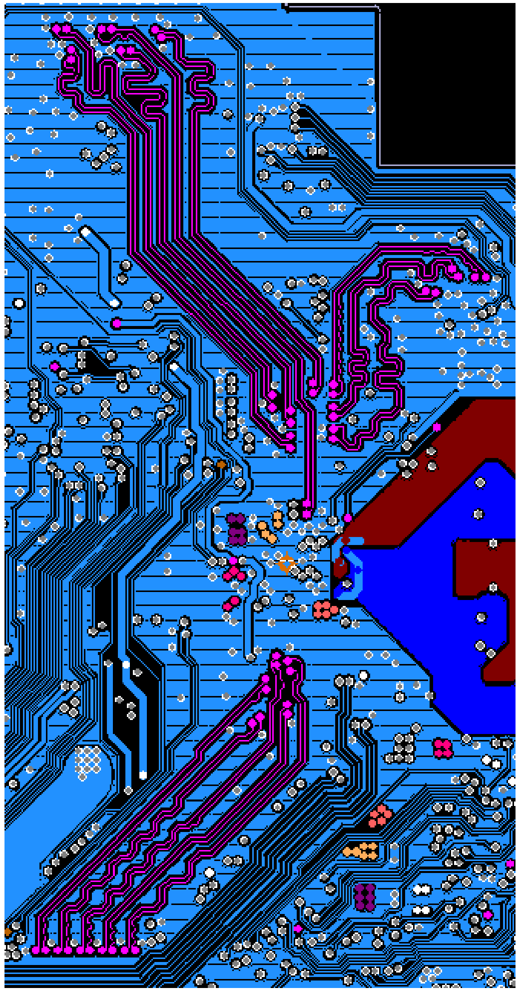


Fig.1

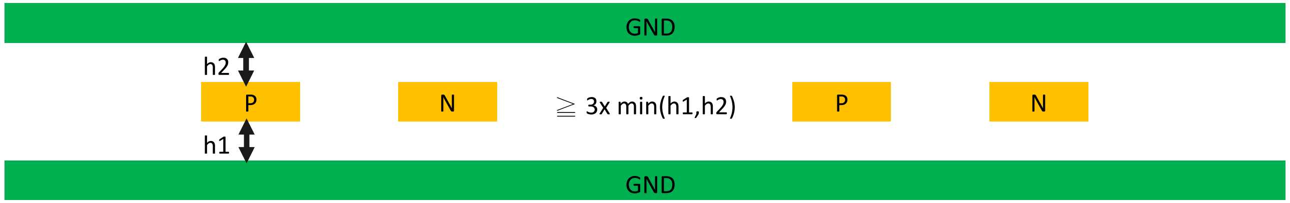
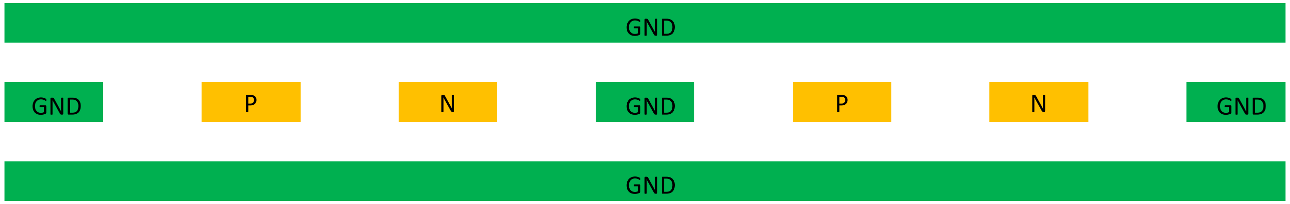


Fig.2



MIPI - CPHY

- MIPI signals' single-end impedance: 50Ω
- Total length < 4 inch (PCB + FPC + Module)
  - Skew in the same trio: 625um
  - Trio-to-trio skew: 22.5mm
- Well shielded by GND (adjacent and up/down layers) is recommended; otherwise keep the spacing ≧ 3x min (h1, h2) rule. (Fig. 1&2)
- Ground isolation (adjacent and up/down layers) from other signals

Fig.1

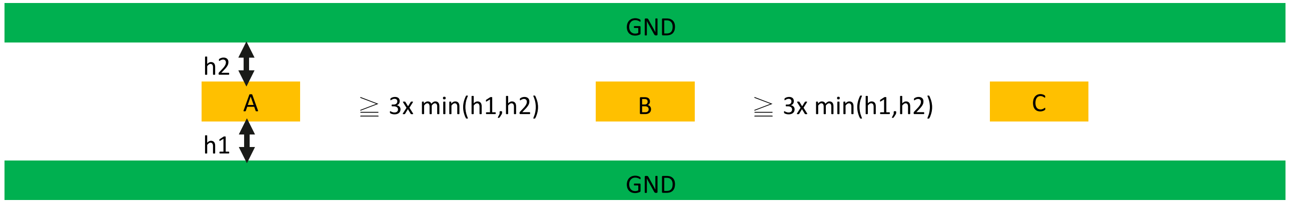
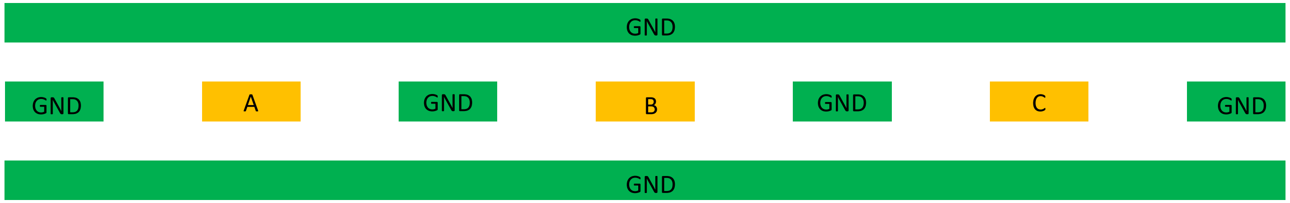
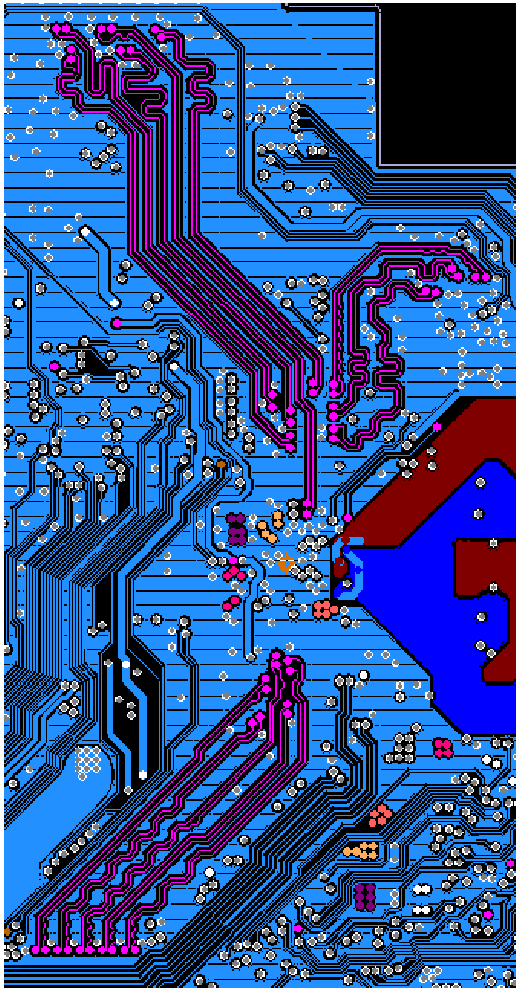


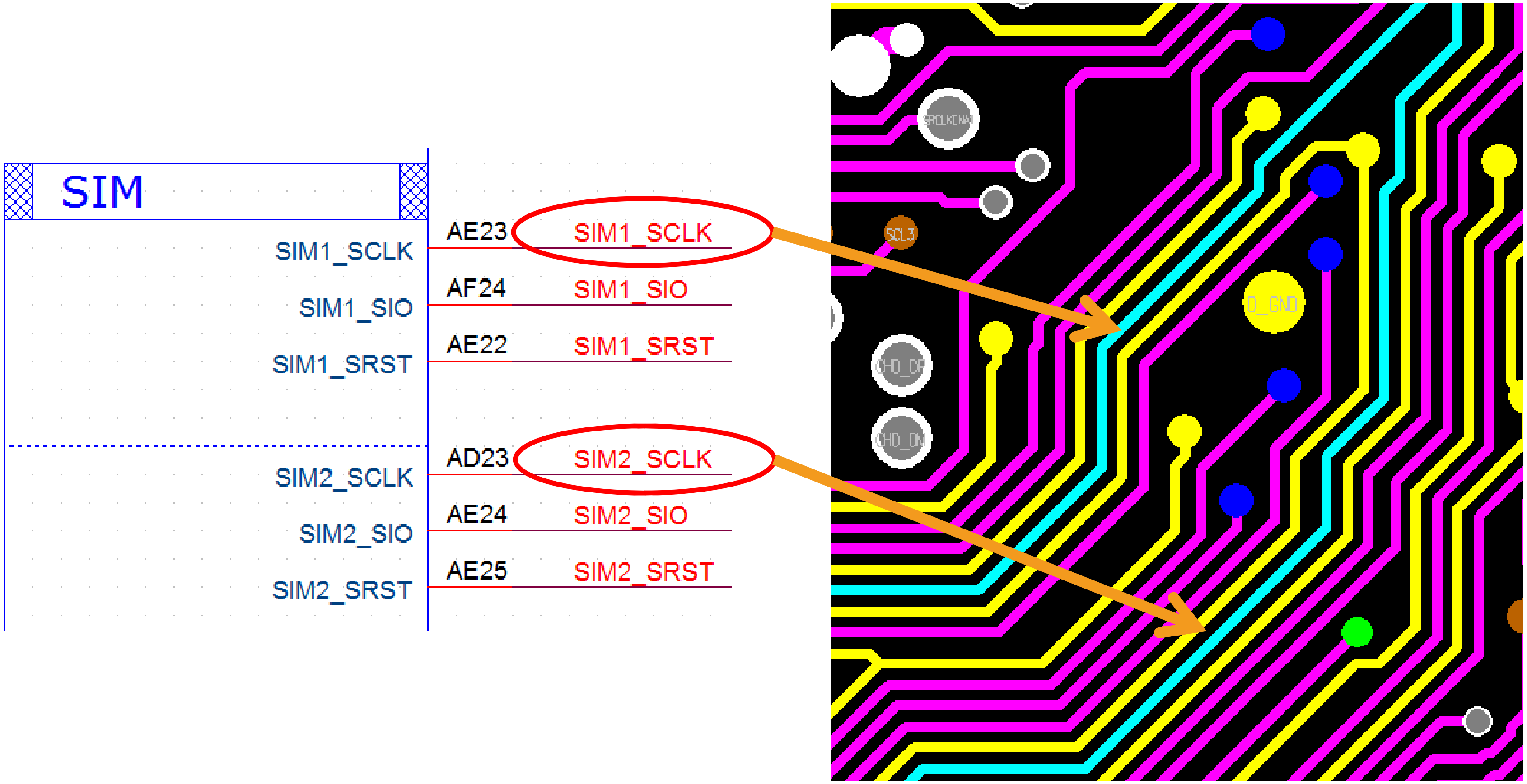
Fig.**2**





SIM Card

- SIM1_SCLK/ SIM2_SCLK should be shielded by GND.



T-CARD

BreakOut Region Topology:

Main routing on L1/L3, **L2/L4 solid reference gnd**:

Breakout length ≦ 5080 um (as short as possible)

A. Keep L2 as solid reference gnd as possible.

B. Place the gnd stitching via between BGA ball and L2 gnd on both AP/eMMC.

C. Trace Width (w) = Minimum Trace Width

D. Trace Spacing ≧ W um

Main Route Region Topology:

Main routing on L1/L3, **L2/L4 solid reference gnd**:

Trace length <= 101600 um

A. Trace Width (w) = W um

B. Trace Spacing:

1. DATA to DATA ≧ 1xW um, 4 trace shielding w/gnd
2. CLK shielding w/gnd on both side
3. CMD shielding w/gnd on both side

Length matching:

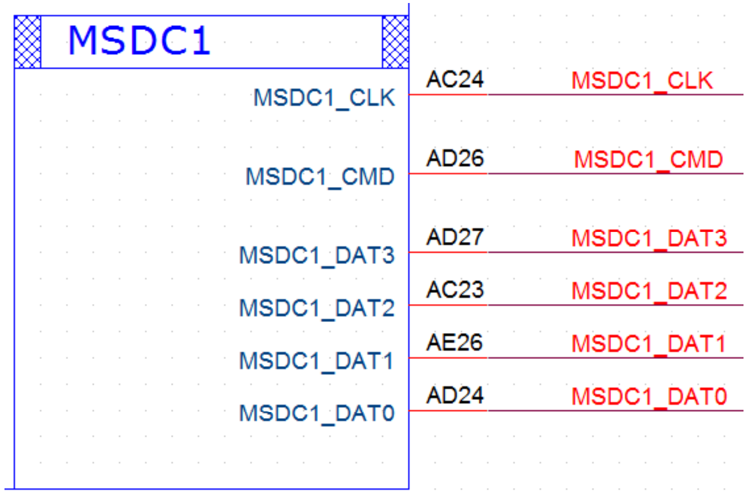
A. |Clock – Data/CMD| ≦ 7620 um

PI : PCB Decap location

A. Distance to SOC ≦ 3810 um

B. Trace width (W) ≧ 200 um

C. Cap Value ≧ 0.1 uF



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ADCT

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